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VHDL Implementation of FM1-Manchester Encoder for DSRC Applications

Remy K.O[1], Manju V.M[2], Suvitha P.S[3]

[1]PG Scholar, [2,3]Assistant Professor,
[1,2,3]Department of Electronics and Communication, IES College of Engineering, Thrissur, India.
remyko37@gmail.com[1],manjuuvm@gmail.com[2],suvithaps@gmail.com[3]

Abstract**:** *The line codes are used for variety of applications. The code diversity between various codes seriously limits the potential to design a fully reused VLSI architecture. In general FM0 – Manchester codes are used for encoding. In this paper, FM1 is used instead of FM0 code. The result shows that the FM1 code is a best alternative choice for FM0 code used in conventional dedicated short range communication. It shows the possibility of replacing a code with another one.*

Keywords**:** *DSRC, VLSI, HUR*

1. Introduction

Dedicated Short Range Communication is a type of Vehicle Safety Communication technologies which offers the potential to effectively support vehicle-to-vehicle and vehicle-to-roadside safety communications. DSRC adopts the methods which increase the overall safety of vehicles. The system architecture of DSRC transceiver is shown in Figure 1.The transmission and reception are represented by upper and bottom parts respectively.

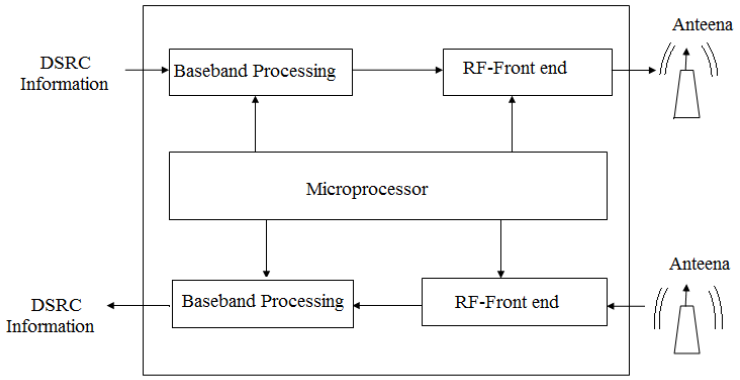

Figure.1 System architecture of DSRC system

The DSRC transceiver is classified into three basic modules they are microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The modulation, clock synchronization, error correction are done by baseband processing. The RF front-end transmits and receives the wireless signal through the antenna. DSRC can be also used in high vehicle speed mobility conditions and they are designed to perform under extreme weather conditions like rain, fog, snow, etc. [1, 3, 4, and 11].

Mohanraj S and Dr.sudha S. Propose a low power VLSI architecture of encoder for downlink applications. In this paper the authors develop encoder VLSI architecture and the performance is compared with existing techniques in terms of power and area. In addition to FM0 and Manchester encoding techniques FM1 and Differential Manchester encoding techniques is proposed in this paper [1]. Triveni A Patil and Sadhana Choudhary propose a fully reused VLSI architecture of FM0 and Manchester code that can be used for memory application. By using FM0/Manchester encoding technique the data will be secure; this process is easy and faster to carry out. Results shows that the architecture is very much effective in secure transmission and operations are faster and easy to perform [2].

Raghavan V proposes an efficient area utilization of FM0, Manchester and Miller encoding architecture for DSRC applications. Originally DSRC applications need FM0 and Manchester codes. By analysis, the authors found that an effective utilization is more which leads to substantial area consumption [4]. The Yu-Hsuan Lee and Cheng-Wei Pan propose a system based on Similarity based logic simplification. It consists of two methods known as area compact retiming and balance logic operation sharing [5].

Daniel Jiang, Vikas Taliwal, Andreas Meier, Wieland Holfelder, Ralf Herrtwich proposed a Design of 5.9GHz DSRC-based Vehicular Safety Communication. This paper provides an overview of DSRC based vehicular safety communications and proposes a coherent set of protocols to address these requirements [6]. S.M.Subramanian, N.Nagaraj, R.Ajin and J.Rasathi proposed a method to find out Power reduction in the VLSI architecture of FM0 and Manchester encoding. The main objective of this work is to combine the VLSI architecture of FM0 and Manchester encoding so that it reduces the power used, by reducing the number of components used and improves the performance of FM0 and Manchester encoding [8].

A new Manchester code generator designed at transistor level is presented in paper [9]. This generator uses 32 transistors and has the same complexity as a standard D flip-flop. It is intended to be used in a complex optical communication system. The main benefit of this design is to use a clock signal running at the same frequency as the data. Output changes on the rising edge and falling edge of the clock. Simulations results show a correct behavior up to 1 Gbit/s data rate with a 0.35 μ CMOS technology within a commercial temperature range [9]. In DSRC the data is transmitted as arbitrary binary sequence. Generally FM0 and Manchester codes are used for this purpose. I'm here aimed to investigate the possibilities of using FM1 and Manchester code for dedicated short range communication and thereby to develop a completely reused system and increase the component utilization and efficiency.

2. System Design

The FM1 and Manchester coding principles are as follows,

2.1 Manchester Encoding

Manchester encoding is also called phase encoding. It can be used for higher operating frequency. Manchester encoding is very common method and is probably the most commonly used.

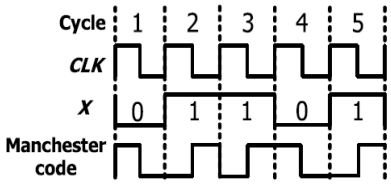

Figure.2 Manchester code

In Manchester encoding the average power is always the same, no matter what data is transmitted. The codes always produce a transition at the center of bit.Here logic '1' is represented by transition from HIGH to LOW. Logic '0' is represented by transition from LOW to HIGH. The operation of Manchester coder is an exclusive OR of the input signal with clock signal[5,6,7,11].

2.2 FM1 Encoding

A transition occurs at the beginning of each clock cycle. A binary "1" is represented by an additional transition at the middle of the clock cycle and binary "0" is represented by no transition at the middle of the clock cycle. Here, the signal to be transmitted done according to the following rules,

- If X (input) is the logic-0, no transition is allowed
- If X (input) is the logic-1, the FM1 code must exhibit a transition
- The transition is allocated among each FM1 code no matter what the X (input) is

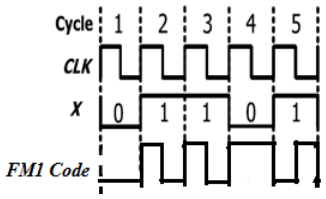

Figure.3 FM1 Code

2.3Analysis of Codes

The Manchester code can be easily realized using XOR gate. The FSM of FM1 code is given below. And from the below diagram, transition table for the code is derived and it represents possible input combinations.

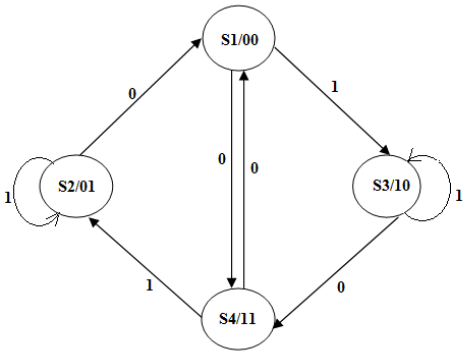

Figure.4 FSM of FM1 Code

TABLE I. Transition table of FM1 code

Present State	Next State	
	Input = 0	Input = 1
S_1	S_4	S_3
S_2	S_1	S_2
S_3	S_4	S_3
S_4	S_1	S_2

The state codes A and B are assigned to each state in the transition table and present states are represented by A(t-1) and B(t-1).The next states are represented by A(t) and B(t) .

TABLE II. State table of FM1 code

Present state		Next state			
A(t-1)	B(t-1)	Input = 0		Input = 1	
		A(t)	B(t)	A(t)	B(t)
0	0	1	1	1	0
0	1	0	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1

An improved state table is derived from the above table as follows; here input is represented as 'x'

TABLE III.Improved State table of FM1 code

Present state		Next state			
A(t-1)	B(t-1)	A(t)		B(t)	
		X=0	X=1	X=0	X=1
0	0	1	1	1	0
0	1	0	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1

A (t) and B (t) can be derived in terms of input, A (t-1) and B (t-1) from this table.

A (t) = NOT B (t-1) (1)

B (t) = X *XNOR* B (t-1) (2)

The hardware architecture for FM1 and Manchester code can be derived from the above two equations. The system consists of separate Manchester and FM1 logic. The Manchester code can be derived from the XOR operation of input and clock. The FM1 logic consists of two D flipflops for storing state codes. By the application of clock signal through a multiplexer is used to select the state codes simultaneously. The output consists of both FM1 and Manchester codes by a signal known as mode through the use of multiplexer.

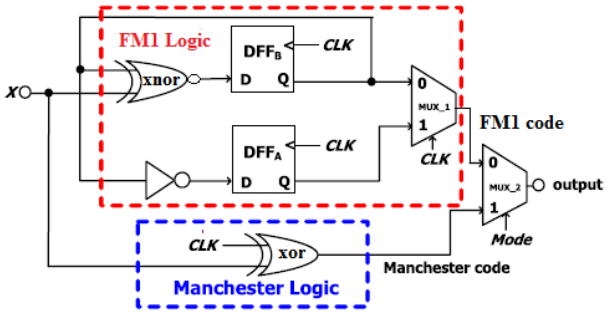

Figure.5 System architecture

3. Hardware Utilization Ratio

HUR is defined as the ratio of active components to the total component in percentage. The component is defined as hardware which performs a specific logic function. The active components mean the components which are present in the implementation of both codes. Total components are the number of components in entire system. The total transistor count can be calculated by counting the transistors used to implement the components used in the circuit. CMOS technology is adopted here.

Table IV .HUR of architecture

code	Active component (Transistor count) / Total component (Transistor count)	HUR
Manchester	2 (42) / 7 (132)	31%
FM1	6 (110) / 7 (132)	83%
Average	4 (46) / 7 (132)	57%

From the table, we can see that the entire system make use of four components on an average. For the designing of an effective system we have to utilize all the available components.

4 .Results And Discussion

The system is implemented in Xilinx ISE Design Suite 14.2 using VHDL language. Mixed style of modeling is adopted here. Here we can reduce the number of signals used in a program and make program very simple and effective by adopting mixed style of modeling. Here, within the same architecture body, we can make use of concurrent statements, sequential statements and interconnected structures. The output can be selected by continuous selection of a and b. Here we make use of three signals a, b and q.

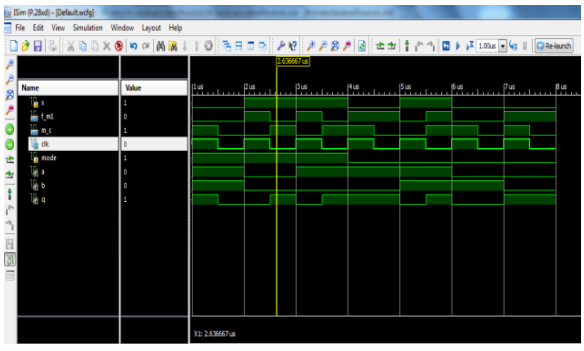

Figure.6.Architecture for FM1 and Manchester codes

Register Transfer Level, or RTL design lies between a purely behavioral description of the desired circuit and a purely structural one. An RTL description describes a circuit as registers and the sequence of transfers between the registers but does not describe the hardware used to carry out these operations. The RTL view of the system provides idea about the number of components and interconnections between them. An RTL design is composed of Registers and combinational function blocks. Here the RTL consists of flipflop, multiplexer and various gates.

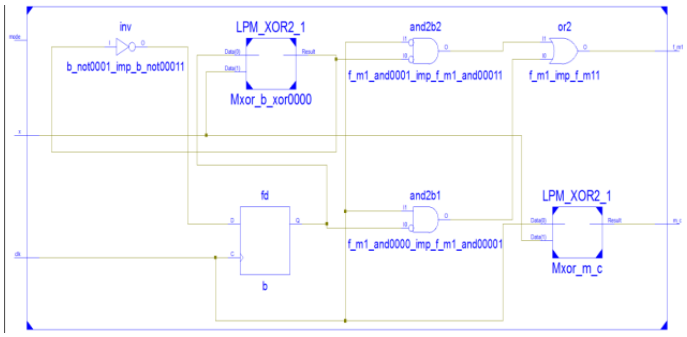

Figure.7. RTL view of Architecture for FM1 and Manchester codes

Conclusion

In this paper, a FM1 and Manchester encoding is proposed and result is obtained. From results we can see that, we need to increase the hardware utilization rate. The techniques can be used for this purpose. The studies shows that , encoder and decoder is not established until now, in future we can make the decoder for the FM1 and Manchester codes and check the reliability and performance of decoder. The FM1/Manchester encoder-decoder pair will be a best alternative choice for FM0/Manchester encoder-decoder pair.

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About Authors

Remy K O, currently pursing PG in VLSI Design from IES college of Engineering, Thrissur, Kerala, India. She received her B.Tech in Electronics and Communication Engineering from Thejus Engineering college, Thrissur, kerala , India in 2015.Her interested research areas are low power VLSI design and digital system design.

Ms. Manju V M, currently working as a Assistant Professor/PG coordinator in Department of Electronics and Communication Engineering at IES College of Engineering, Thrissur, Kerala, India. She received her M.E degree in VLSI Design from Anna University, Trichi in 2009. She is a member of ISTE and IEEE. Her interested research areas are low power VLSI design and digital system design.

Ms. Suvitha P.S. currently working as Assistant Professor in Department of Electronics and Communication Engineering at IES College of Engineering, Thrissur, Kerala, India. She received her B.Tech degree in Electronics and Communication Engineering from MG university in 2008 and M.Tech. degree from Calicut university in 2014. Her a interested research area is digital system design.