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Study on Spurious Power Suppression Technique in Distributed Arithmetic Based DWT Filter Bank

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Abstract: *Discrete wavelet transform is a fundamental block in several schemes for image compression. The implementation requires filter banks that uses multiplications leading to a high hardware complexity. Hence using Distributed arithmetic which is a general and effective technique to implement multiplierless filter banks has already exploited to implement the discrete Wavelet transform. This work proposes a general method to implement a discrete wavelet transform architecture based on power suppressed and result biased distributed arithmetic to produce approximate results. The novelty of the proposed method relies on the use of result biasing techniques and spurious power suppression technique. Compared with previously proposed distributed arithmetic based architectures, this technique saves power at the expense of very small area augmentation.*

Keywords *—Distributed Arithmetic, DWT, FIR filter bank, JPEG2000, Spurious Power Suppression Technique, Sub Expression Elimination.*

1. Introduction

In the last few years discrete wavelet transform has gained a wide impact in audio and image processing. The rapid progress of VLSI design technologies, many processors based on audio and image signal processing have been developed nowadays. The two-dimensional discrete wavelet transform plays a major role in image/video compression standard, such as JPEG2000 [1-2]. As wavelets decompose the signal at one level of approximation and detail signals at the next level [3-4], subsequent levels add more details to the information content. Presently, research on the DWT is attracting a great deal of attention in many areas, such as computer graphics, numerical analysis, radar target distinguishing etc. The architecture of the 2D DWT is mainly composed of the multi-rate filters which require high complexity hardware especially multipliers. Hence for the practical applications in digital cameras a high efficiency low cost hardware is impossible. Many low complexity and multiplierless architectures were exploited in recent years. Among them are the B-spline factorization [5], [6] exploited to design multiplierless filter bank architectures, algebraic integer quantization [7], [8], coefficient rationalization [9], polymorphic implementation [10], and half-band polynomial factorization [11]. Unfortunately, all the above said techniques require not only knowing the value of the filter taps but also the mathematical derivation of the filters or at least some specific factorizations. An indirect method based on row-column decomposition is explored which is the basis of distributed arithmetic. Distributed arithmetic (DA) was proposed about two decades ago and has since used widely in VLSI implementations of DSP architectures where multiplication and/or addition is the predominant operation. The distributed arithmetic approach speeds up the multiply process by pre-computing all the possible medium values and storing these values in a ROM. The input data can then be used to directly address the memory and the result. But the major drawback of this approach is the exponential growth of ROM size with the number of inputs and internal precision. Hence a modified approach using DA where DWT coefficients inner product is distributed

over the input as one employed in architecture for computation of low complexity and high throughput architectures of DCT [12], [13], FIR filter [14], [15], multiplierless FB implementations of the DWT [16] [17] improvement of 77.6% over filter based and 40.27% over lifted based architectures, result biased DA based architecture [18]. In this paper, we propose to replace the ripple carry adders with a spurious power suppression to reduce the power dissipation and combinational time complexity of the circuit; we propose a spurious power suppression technique [19] to DA based architecture [18]. In the proposed SPST logic design, the adders in the transform coding design are separated into two parts, i.e., the most significant part and least significant part and turns off the MSP when it does not affect the computation results to save power. Besides, detection logic and SE units are introduced to determine the effective ranges of the operands and compensate for the sign signals of the MSP, respectively. This action is realized easily by controlling the three bit output of the detection logic unit with extremely small cost. The paper is structured as follows. Section II summarizes the general computational scheme of DA-based architectures for wavelet filters and Section III explains the spurious power suppression technique. In Section IV conclusions are drawn. In Section V references are mentioned.

2. DA-Based Architecture for the 9/7 Wavelet

DA based architecture consist of a butterfly circuit made of adders, a hardwired shifted network and a tree adder for adding the partial results. CDF 9/7 filter is considered here with 9 coefficients in the low pass h[j] and 7 coefficients in the high pass g[j] region as shown in table 1.

Table I. Wavelet coefficient (9/7) expressed in binary and showing common terms.

-r	*h[±4]*	*h[±3]*	*h[±2]*	*h[±1]*	*h[0]*	$\underline{d}_j$	*-g[±3]*	*-g[±2]*	*-g[±1]*	*-g[0]*	$\underline{d}_j$
0	0	1	1	0	0	$\underline{d}_0$	1	0	0	1	$\underline{d}_6$
1	0	1	1	0	1	$\underline{d}_3$	1	0	0	0	$\underline{d}_9$
2	0	1	1	1	0	$\underline{d}_8$	1	0	1	1	$\underline{d}_{11}$
3	0	1	1	0	0	$\underline{d}_0$	1	0	0	1	$\underline{d}_6$
4	0	1	0	0	1	$\underline{d}_6$	1	0	0	1	$\underline{d}_6$
5	0	1	1	0	1	$\underline{d}_3$	0	0	1	0	$\underline{d}_{12}$
6	1	0	0	1	0	$\underline{d}_4$	1	1	0	0	$\underline{d}_0$
7	1	1	1	0	1	$\underline{d}_2$	0	1	1	0	$\underline{d}_{10}$
8	0	1	1	0	0	$\underline{d}_0$	0	1	1	1	$\underline{d}_5$
9	1	1	1	0	0	$\underline{d}_1$	0	0	1	0	$\underline{d}_{12}$
10	1	0	1	1	1	$\underline{d}_7$	1	1	0	1	$\underline{d}_3$
11	0	1	1	0	0	$\underline{d}_0$	0	0	1	0	$\underline{d}_{12}$
12	1	0	1	1	1	$\underline{d}_7$	1	1	0	0	$\underline{d}_0$

For convenience we consider h[j] and –g[j] instead of h[j] an g[j] so as to find out more common terms and have common subexpression elimination. To make the coefficients compatible with open jpeg model, we choose the h[j] and g[j] taps as one bit for integer part and 12 bits for fractional part. Hence coefficients are rounded to 13 decimal places. From the table 1, it is clear that the coefficients are symmetric in nature. The repeated common terms are grey shaded in similar manner. To have filter symmetry, the column vectors are arranged as

$$C_\omega = \begin{cases} x[i]\omega = 0 \\ x[i+\omega] + x[i-\omega]\omega = 1,2,3,4 \end{cases} \qquad (1)$$

Where $x[i]$is the i-th input applied C_ω is combined with 13 $\underline{d}_j$ values hence forming a butterfly circuit as in figure 1(a). Inputs are given serially and stored in the register shifted at successive clock pulses. Thus the computations for the input say for example x[i-ω] and x[i+ω] (which should be actually computed six clock pulse hence) can be computed together. The adder used are normal ripple carry adders. Twenty seven adders, two negation block, fourteen 2:1 multiplexers and twelve shifting network, eight delay elements are employed. This causes the increased delay and power. Software building is made on Xilinx platform using verilog HDL coding.

The appropriate low pass and high pass filters are terms are selected using a Hi-Lo signal to the multiplexer. They are shifted and then added together at tree adder as shown in figure 1(b). For the 13 dj.c values, 13 shifts from 0 to 12 are applied (division) by the hardwired shifted network.

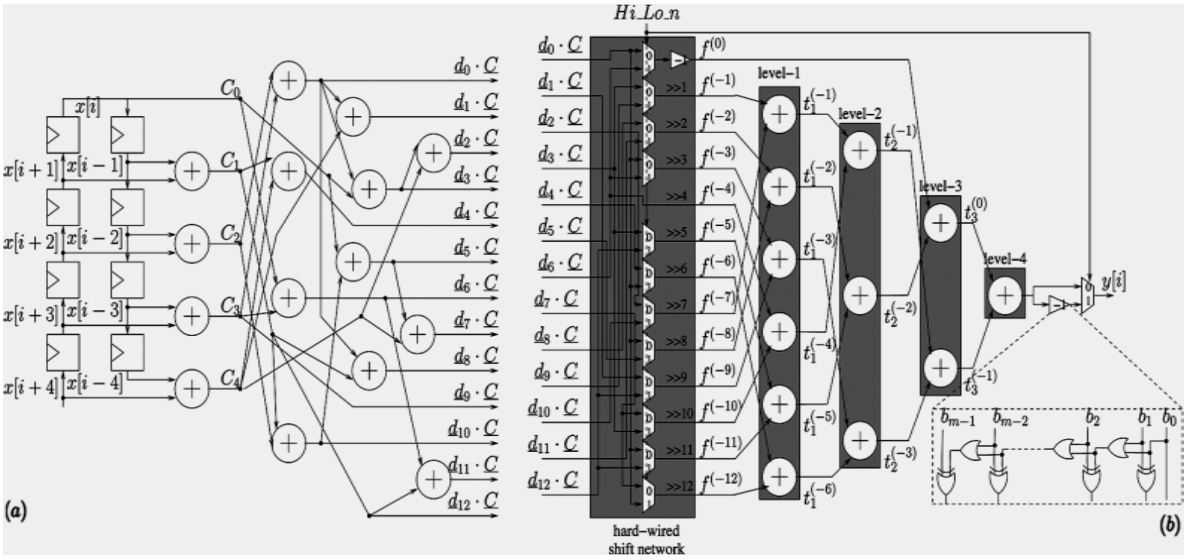

Figure 1. Butterfly circuit (a) and tree adder with hard-wired shift network computational scheme (b)

Moving on to the tree adder, the addition takes place in a fashion as below.

$$t_1^{(-i)} = f^{(-i)} + f^{\left(\frac{-n}{2} - i\right)} \qquad (2)$$

In equation (2) as the second term in the RHS is very small, hence probability based result biasing [18] is applied to achieve reduced power consumption. At the final stage, the low pass and high pass output are obtained as the output of multiplexer with select line Hi-Lo_n. The high pass output are obtained by taking the twos complement as it was already negated at the start to have more common expression terms.

2. Spurious Power Suppression Technique

The result biased DA based DWT utilizes more than 25 adders for the implementation of 9/7 wavelet filter bank. The adder used here is ripple carry adder which utilizes more delay and power. With the help of spurious power suppression technique, these ripple carry adders are replaced using a low power adder. We aim to reduce about dynamic power consumption with a very little area augmentation. The proposed adder splits the input arriving to it into two parts. One least significant part (LSP) and other most significant part (MSP). Different cases have to be mentioned where the proposed adder is applicable. These special cases either have the MSB bits either as all ones or as all zeros. Whose value can be predetermined and can be avoided from calculating. The first case illustrates a transient state in which spurious transitions of carry signals occur in the MSP, although the final result of the MSP is unchanged. Meanwhile, the second and third cases describe situations involving one negative operand adding another positive operand without and with carry-in from the LSP, respectively. Moreover, the fourth and fifth cases demonstrate the addition of two negative operands without and with carry-in from the LSP, respectively. In those cases, the results of MSP are predictable; therefore, the computations in MSP are useless and can be neglected. Eliminating those spurious computations not only can save the power consumption inside the adder/subtractor in the current stage but also can decrease the glitching noises which cause power wastage inside the arithmetic circuits in the next stage. Fig. 2 shows a 16-bit adder/subtractor design example adopting the proposed SPST. In this example, the 16-bit adder/subtractor is divided into MSP and LSP between the eighth and the ninth bits.

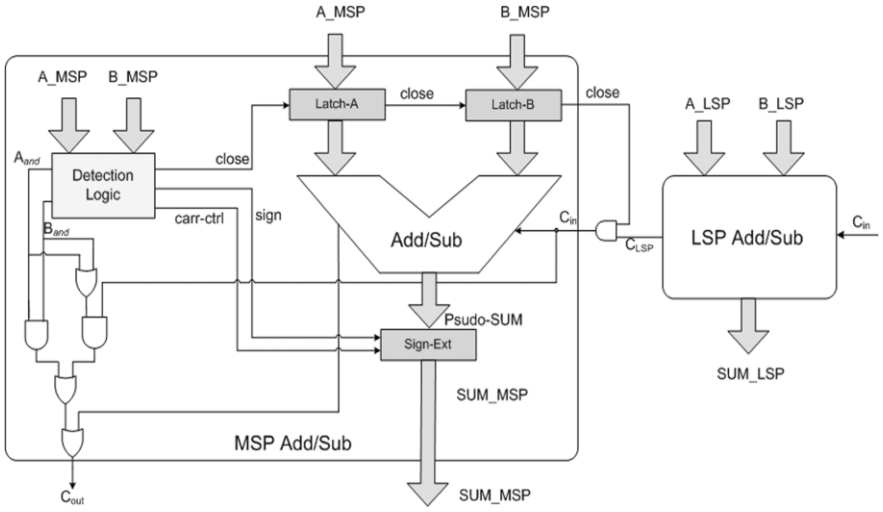

Figure 2. Architecture of SPST adder.

Latches implemented by simple AND gates are used to control the input data of the MSP. When the MSP is necessary, the input data of MSP remain unchanged. However, when the MSP is negligible, the input data of the MSP become zeros to avoid glitching power consumption. The two operands of the MSP enter the detection-logic unit, except the adder/subtractor, so that the detection-logic unit can decide whether to turn off the MSP or not. Based on the detection-logic unit of SPST is shown in Fig. 3 which can determine whether the input data of MSP should be latched or not.

Moreover, we propose the novel glitch-diminishing technique by adding three 1-bit registers to control the assertion of the *close*, *sign*, and *carr-ctrl* signals to further decrease the transient signals occurred in the cascaded circuits which are usually adopted in VLSI architectures designed for multimedia/DSP applications.

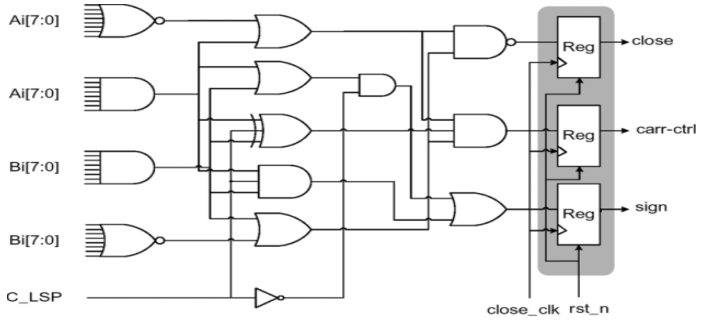

Figure 3. Detection logic design

Fig. 3 shows the data-controlling components of the SPST, where Fig. 4 shows the design of the data latch. The inputs are loaded to the adder only when close signal is high else the inputs at adders are zeros and partial sum produced from adders are zeros and output is calculated from sign extension circuit.

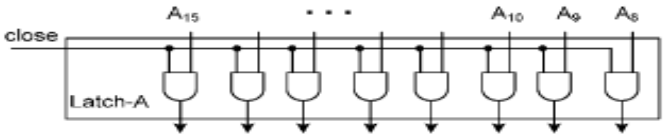

Figure 4. Data latch design.

The SE circuits can be intuitively implemented by multiplexers to compensate for the sign signals of the MSP, as shown in Fig.5. The input data of the SE circuits are pseudo summations (PS) from the MSP adder/subtractors.

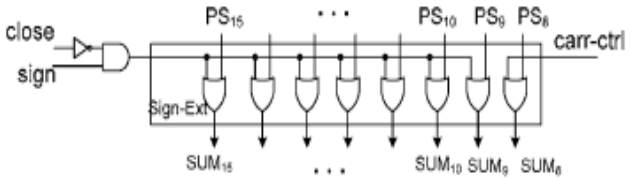

Figure 5. Sign extension unit design.

4. Conclusion

Discrete wavelet transform based image compression is very effectively trending nowadays. The project helps in bringing out an efficient way to reduce power consumption in the existing result biased distributed arithmetic based filter architectures for approximately computing DWT. The limitation is that we need to compromise the area occupied. The ripple carry adders in the above said paper are replaced using a spurious power suppression technique based adder expecting to reduce power dissipation. Exploring a comparative study on the paper is in advance. SPST technique is studied and researched. Base paper work is studied. Coding integration and comparison is progressing. As an advancement of the project more optimization of XOR gates can be done. This project has wide application in signal and image processing, biomedical applications including QRS peak detection signal denoising and image compression etc.

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