Indian Journal of Emerging Electronics in Computer Communications
Vol.4, Issue 1 (2017) Page.638-643
ISSN: 2393-8366

Study on Area Efficient Radix-2 FFT Architecture to Process Twin Data Streams for High Speed Real Time Application

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Abstract: *This paper proposes a novel shared multiplier scheduling scheme for area efficient radix-2 FFT architecture to process twin data streams for High speed real time application. In these days many application require simultaneous computation of multiple independent Fast Fourier Transform with its outputs are in natural order. So this paper present a 16 point pipelined FFT processor for FFT computation of two independent data stream. In this N/2 decimation in time FFT and N/2 point decimation in frequency FFT to process the odd and even samples of two data streams separately. This SMSS technique reduce total number of complex multiplier and hardware complexity. The proposed pipelined FFT processor based on SMSS are designed using XILINX ISE TOOL and coded by Verilog HDL language. In addition the proposed processor can be extended to any FFT sizes using additional stages.*

Keywords *- SMSS, Radix 2 pipelined FFT, DIT and DIF, Multipath delay commutator, Odd and Even samples, MIMO, Xilinx ISE Tool.*

1. Introduction

FFT Processor play an important role in OFDM techniques, image processing and signal processing application. Such application require high speed FFT Processor to meet demands for higher data rates. For implementing such processors several architectures are used. They are Memory based, Reconfigurable and Pipelined FFT. Memory based FFT processor [1], [2] are used to achieve small area. Here it use Application specific instruction set processor to meet flexibility for FFT computation. Reconfigurable FFT processors [3] are used to select various FFT sizes on processor so it will reduce hardware complexity. The pipelined processors [4] are used for achieving high throughput rate. Pipelined processors are classified into single path delay commutator (SDC), single path feedback (SPF), Multi path delay feedback (MDF) and multipath delay commutator. This architecture is based on Multipath delay Commutator. MDC architectures provides high throughput rate and simple synchronizing control using multi data path. In MDC Radix size is high then throughput is high.

FFT architectures [5]–[8], In which multiple independent data streams are used. However, all the data streams are processed by a single FFT processor in [5] and [8]. In [8], four independent data streams are processed one by one. Similarly, eight data streams are processed at two domains in [5]. Thus, the outputs of multiple data streams are not available in parallel. In order to simultaneously process the data streams, more than one FFT processors need to be employed. In [6], one to four data streams are processed using multiple data paths for wireless local area network application. Data of different data streams are interleaved to process them simultaneously in [7].

The modified architecture is 16 point pipelined FFT Processor based on shared multiplier scheduling scheme. In [9] it process two different data streams concurrently with less amount of hardware. The odd inputs, which are in natural order, are bit reversed first and then they are

processed by N/2-point decimation in time FFT. The even samples are directly processed by N/2-point DIF FFT. So its outputs are bit reversed order. Therefore, the outputs of N/2-point DIF FFT are bit reversed. Outputs of the two N/2 point FFTs are further processed by the two parallel butterflies to generate the outputs of Npoint FFT in natural order. In FFT computation several multiplications are required. These multiplications are performed by SMSS technique. Here bit reversing is carried out by the scheduling registers. Which are actually used to delay the samples for performing the butterfly operations. Thus, FFT architecture does not use any dedicated circuit to bit reverse the data. Because of this, the proposed architecture requires less number of registers than the prior FFT designs.

2. Fast Fourier Transform

The FFT is an algorithm to speed up the DFT calculation by reducing the number of multiplications and additions required. It has several applications in signal processing. Because of the complexity of the processing algorithm of FFT, now various FFT algorithms are available for processing function and to reduce hardware complexity. Here the FFT processor is to perform 16 points FFT analysis.

The Fourier transform converts information from the time domain into the frequency domain. It is an important analytical tool in such diverse fields as acoustics, optics, seismology, telecommunications, speech, signal processing, and image processing.

There will be two classes of FFT operation

1) Decimation in Time (DIT) Algorithm
2) Decimation in Frequency(DIF) Algorithm

In DIT, The N point DFT of sequence X(n) convert the time domain N point sequence X(n) to Frequency domain N point sequence X(k).In DIT Algorithm the time domain sequence X(n) is decimated and smaller point DFT are performed. The result of smaller point DFTs are combined to get the result of N point DFT.

In DIF, In DIF algorithm the frequency domain sequence X(k) is decimated. In this algorithm the N point time domain sequence is converted to two numbers of N/2 Point sequence. Then each N/2 point sequence is converted to two numbers of N/4 point sequence. Thus we get 4 numbers of N/4 point sequence. This process is continued until we get N/2 numbers of 2 point sequences. Finally the 2 point DFT of each 2 point sequence is computed. The 2 point DFTs of N/2 numbers of 2 point sequences will give N samples, which is the N point DFT of the time domain sequence.

3. Existing 16-Point Radix-2 FFT Architecture

The architecture is designed to process two independent data streams simultaneously with less amount of hardware. The odd inputs, which are in natural order, are first bit reversed and then they are processed by N/2-point decimation in time (DIT) FFT. The eve samples are directly processed by N/2-point DIF FFT, so its output are in bit reversed order. Therefore, the outputs of N/2-point DIF FFT are bit reversed. The outputs of the two N/2-point FFTs are further processed by the two-parallel butterflies to generate the outputs of N-point FFT in natural order. The bit reversing is carried out by the scheduling registers, which are actually used to delay the samples for performing the butterfly operations. Thus, the FFT architecture does not use any dedicated circuit to bit reverse the data. As a result, the proposed architecture requires less number of registers than the prior FFT designs.

There will be two 8 point MDC FFT architectures to process two data streams. The delay commutator units at the left side of SW_1 separate the odd and even samples. The shift registers in the delay commutator units, which receive inputs, are used to bit reverse the odd input samples. These shift registers are called reordering shift registers (RSRs).The RSR in the last stage store outputs from the eight-point DIF FFT and bit reverses them. The BF_2 carries out two-parallel

butterfly operations between the bit reversed data in the RSR in the last stage and outputs from the eight-point DIT FFT. Thus, the upper and lower BF_2 in the last stage generate the FFT outputs of the first and the second data streams in normal order.

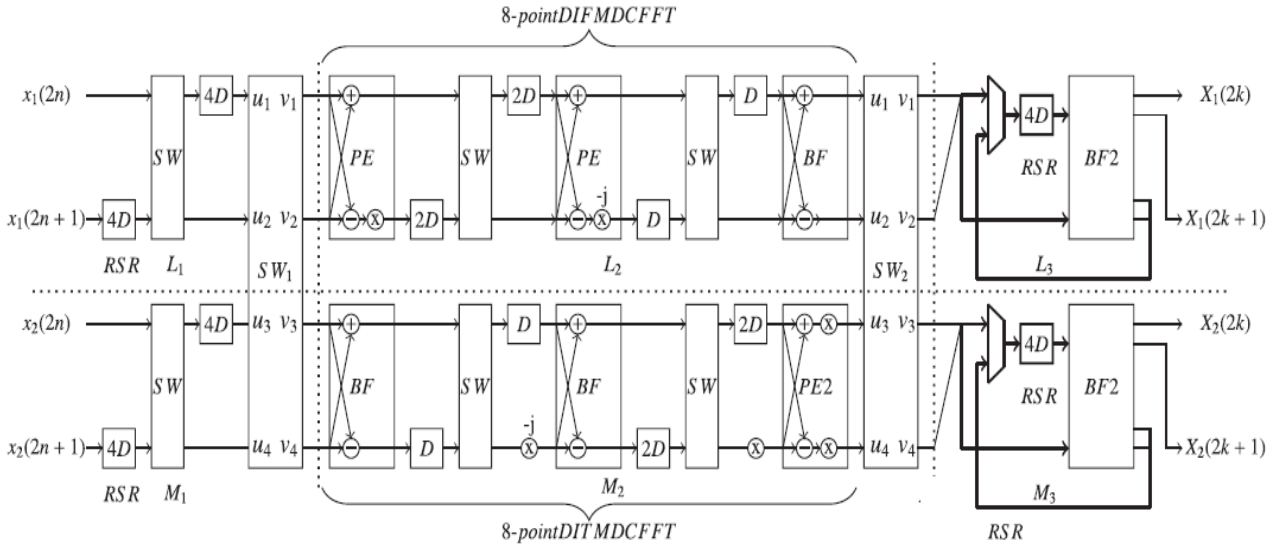

Figure 1: 16 point rAdix 2 FFT architecture

The two data paths from SW_2 are combined together, so the word length of the data path in last stage is twice and so thick lines are used for representing the data paths and registers. The FFT architecture in Fig. 1 is divided into six levels (L_1, L_2, L_3, M_1, M_2, and M_3). The RSR registers in the levels L_1 and M_1 reorder the odd input data and the RSR registers in the levels L_3 and M_3 reorder the partially processed even data. The eight-point DIF and DIT FFT operations are performed in the levels L_2 and M_2, respectively. The data from L_1 and M_1 can be forwarded to L_2 and M_2, respectively, or vice versa with the help of SW_1. Similarly, the data from L_2 and M_2 can be forwarded to L_3 and M_3, respectively or vice versa with help of switch SW2. SW1 and SW_2 have two switches (SW) to swap the data path and propagate the data to different levels. During the normal mode, the switches (SW_1 or SW_2) pass the data at u_1, u_2, u_3, and u_4 to v_1, v_2, v_3, and v_4, respectively.

However, during the swap mode, the switches (SW_1 or SW_2) pass the data at u_1, u_2, u_3, and u_4 to v_3, v_4, v_1, and v_2, respectively. SW_1 is in the swap mode during the first N/2 clock cycles and it is in the normal mode during N/2 + 1 to N. On the other hand, SW_2 is in the normal mode during the first N/2 clock cycles and it is in the swap mode during N/2 + 1 to N. Thus, SW_1 and SW_2 are in different modes at any time and change their modes for every N/2 clock cycles. Moreover, if there is transition of data between L_y and L_{y+1} or My and M_{y+1}, then the switches are in the normal mode, and if there is transition of data between L_y and M_{y+1} or My and L_{y+1}, then the switches are in the swap mode. Like other control signals in the design, the control signals to the switches SW_1 and SW_2 are externally provided and these switch control signals swap at every N/2 clock cycles.

4. Architecture of SMSS Based FFT

The proposed SMSS based 16 point pipelined FFT processor with MDC architecture gives high throughput and low hardware complexity. In the existing processor, the L_2 and M_2 stages consist of several complex multiplication during 8 point DIT and DIF operation. So this stage will increase the hardware complexity. In existing architecture, The multiplication coefficient used in L_2 and M_2 stages are 0.707 ,-1 and 1.In PE_2 both multiplication coefficients are 0.707.So in this stage a SMSS technique is introduced. In the existing processor the multiplication by 0.707 can

employ a bit parallel multiplier according to the equation (1), and the circuit diagram is shown in Fig 2.

$$\text{Output} = \text{in} * \sqrt{2}/2 = \text{in} * [1 + (1+2^{-2})(2^{-6} - 2^{-2})] \text{ ---- (1)}$$

The resulting circuit uses three additions and three barrel shift operations.

The proposed SMSS Architecture is shown in Fig 3. This method is designed based on Mux working. It consist of delay elements that will Store the required multiplication coefficients.

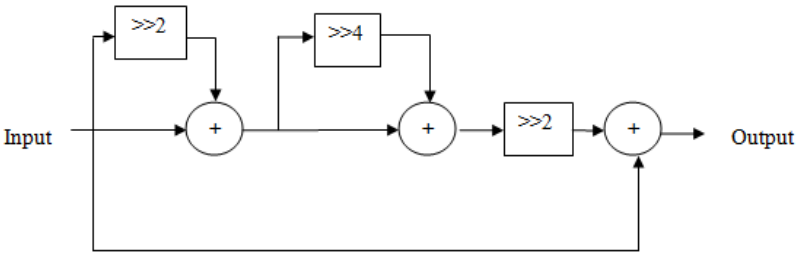

Figure 2: Circuit diagram of the bit-parallel multiplication by $1/\sqrt{2}$

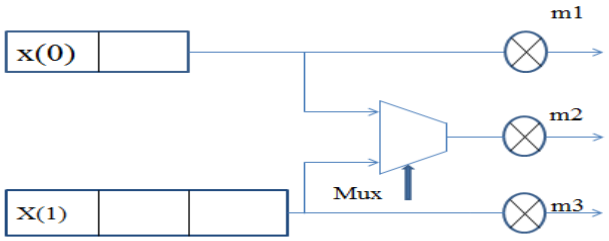

Figure 3: SMSS Architecture

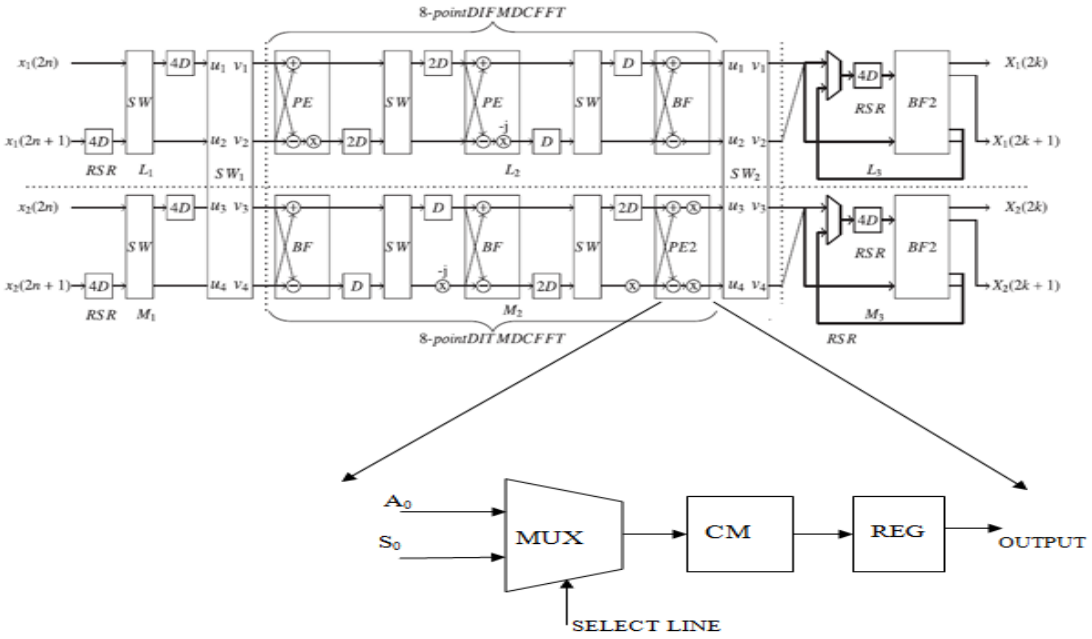

Figure 4: SMSS Based FFT architecture

In proposed method, The SMSS technique is applied in PE_2 stage of Existing processor. Because both adder and subtractor output is multiplied by 0.707 multiplication coefficient. So The adder and subtractor output of PE_2 stage is selected by using shared multiplier scheduling scheme. Then it is multiplied by 0.707 and the output is stored in a register. Therefore by using this technique we can reduce the area, power and time delay of architecture compared to existing processor. The architecture of introduced SMSS based FFT architecture is shown in Fig 4.

5. Conclusion

Here a technique to reduce the area of pipelined FFT architecture is presented. It is designed using Xilinx ISE14.2 Tool. This technique reduce number of complex multiplication and hardware complexity. In which outputs are generated in the natural order. The proposed processor can process two independent data streams simultaneously, Somakes it suitable for many high-speed real-time applications. The bit reversal circuit present in prior designs is eliminated in this technique by integrating two FFT processors. In addition the proposed processor can be extended to any FFT sizes using additional stages.

Acknowledgement

I express my sincere thanks to my guide Ms. Rachana M K for her valuable guidance and useful suggestions, which helped me in the project work.

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