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Voltage Regulation and Reactive Power Compensation Using SA Algorithm

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Abstract—*Voltage regulation and reactive power compensation is one of the most challenging problem in the power systems. It may occur in transmission line of the power system. Due to that generation outages, sudden increase of load demand, or failure of equipment's may happen, which will be rectified using Unified Power Flow Control (UPFC). In this project, minimize the optimization control by using Sinusoidal Pulse Width Modulation (SPWM), PI controller and Simulated Annealing (SA) technique is used to generate firing pulses for both the converters in UPFC. In this study simulations were performed on IEEE 14-bus. Results of simulations are encouraging and could efficiently be employed for power system operations.*

Keywords *– UPFC, SA, SPWM, Voltage Regulation, Reactive power compensation.*

I. Introduction

Today's power systems are highly complex and require careful design of new devices taking into consideration the already existing equipment , especially for transmission systems in new deregulated electricity markets. This is not an easy task in the power system. Thus, this requires a review of traditional methods and the creation of new methods. In the late 1980's, the Electric Power Research Institute (EPRI) introduced a new approach to solve the problem of designing and operating systems. The proposed concept is known as Flexible AC Transmission systems (FACTS). The two main objectives of FACTS are to increase the transmission capacity and control power flow over designed transmission routes. In this project, a Unified Power Flow Control (UPFC) is used. These devices by controlling the power flows in the network without generation rescheduling or topological changes can improve the performance. The control scheme has the fast dynamic response and hence is adequate for improving transient behaviour of power system after transient conditions [1]. A Sinusoidal Pulse Width Modulation (SPWM) is a method for finding a good (not necessarily perfect) solution to regulation of voltage and active and reactive power compensation problem. In fact, a massive number of small power generators are envisioned to be deployed in the low and medium voltage power distribution grid. The integration of the distributed energy resources in the distribution network could yield to a number of benefits for the electrical distribution system, e.g. voltage profile improvements, reduction of line losses, reduction of power generation cost and other ancillary services [2]. Voltage regulation is achieved by controlling the generators reactive power output, mainly because reactive power can be produced almost with no cost and does not withstand to economical issue, as instead the active power does. Traditionally, the voltage control is performed using mechanical control devices, such as shunt capacitor banks or on-load tap changers [3], that often are too slow to respond properly to the voltage fluctuation due to the variability of the energy resources and of the load demand. These are the reasons that lead to the recent interest for strategies

that regulate the voltage magnitudes in the distribution network by acting the injection (or absorption) of the micro-generators reactive power. Many inverters have the capability, when they are running below their rated output current, to inject (or to absorb) reactive power together with active power [4]. In order to provide the voltage regulation and reactive compensation, the micro generates are employed and maintain the constant voltage in the system [5]. The controllers are employed in the FACTs devices like UPFC. The FACTs devices are balancing the load and maintain the voltage in the system [6].

II. Proposed System

In this proposed system, the voltage profile is improved by using FACTs device UPFC (Unified Power Flow Controller). The UPFC operates only under balanced sine wave source. That control signal (or) balanced sine wave source is produced by different types of techniques. Here, we used three different types of techniques. They are SPWM (Sinusoidal Pulse Width Modulation), PI (Proportional Integral) controller, SA (Simulated Annealing) algorithm. The UPFC which is connected to the 8^{th} of the system. The voltage profile of the bus improved compared to the other buses.

2.1 Unified Power Flow Controller

The UPFC is a combination of a static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) coupled via a common DC voltage link. UPFC consist of two back to back converters named VSC1 and VSC2, are operated from a DC link provided by a dc storage capacitor. These arrangements operate as an ideal ac to ac converter in which the real power can freely flow either in direction between the ac terminals of the two converts and each converter can independently generate or absorb reactive power as its own ac output terminal.

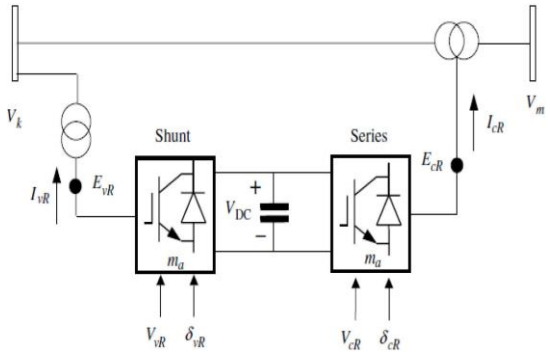

Fig.1.Schematic Diagram of UPFC

One VSC is connected to in shunt to the transmission line via a shunt transformer and other one is connected in series through a series transformer. The DC terminal of two VSCs is coupled and this creates a path for active power exchange between the converters. VSC provide the main function of UPFC by injecting a voltage with controllable magnitude and phase angle in series with the line via an injection transformer. This injected voltage act as a synchronous ac voltage source. The transmission line current flows through this voltage source resulting in reactive and active power exchange between it and the ac system. The reactive power exchanged at the dc terminal is generated internally by the converter. The real power exchanged at the ac terminal is converted into dc power which appears at the dc link as a real power demand. And VSC1 is to supply or absorb the real power demanded by converter2 at the common dc link to support real power exchange resulting from the series voltage injection. This dc link power demand of VSC2 is converted back to ac by VSC1 and coupled to the transmission line bus via shunt connected transformer. In addition, VSC1 can also

generate or absorb controllable reactive power if it is required and thereby provide independent shunt reactive compensation for the line. Thus VSC1 can be operated at a unity power factor or to be controlled to have a reactive power exchange with the line independent of the reactive power exchanged by VSC1. Obviously, there can be no reactive power flow through the UPFC dc link.

2.2 UPFC using SPWM method

In this method, the PWM generator is directly connected to the UPFC. PWM generator compares sinusoidal wave to the triangular wave. It gives the control signal to the UPFC.

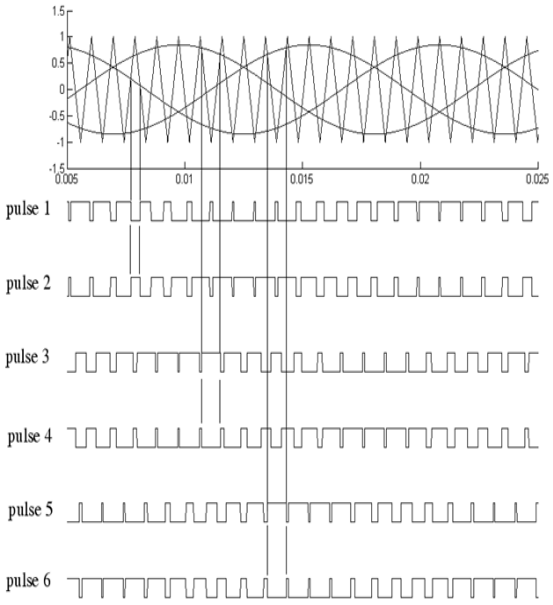

Fig.2. PWM signal generation

The rms ac output voltage,

$$V_o = V_s\sqrt{\frac{p\delta}{\pi}} \rightarrow V_s\sqrt{\sum_{m=1}^{2p}\frac{\delta_m}{\pi}}$$

Where, p=number of pulses

δ= pulse width

Fig.2. shows the PWM generation of the UPFC. The PWM signal through simply noting the intersections between a sawtooth (or) triangular trigger signal and a reference sinusoid. The length of the pulses is dependent upon the intersection of the reference sinusoid and trigger signal. When the sinusoid is greater than the signal, the PWM pulse is switched to the on/high position. When the sinusoid is less than the signal, the PWM pulse is switched to the off/low position.

2.3 UPFC using PI controller method

The PI control scheme is named after its two correcting terms, whose sum constitutes the manipulated variable (MV).

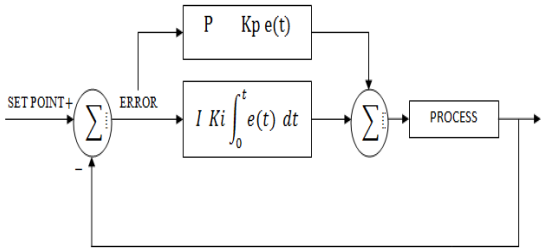

Fig.3.Schematic diagram of PI controller

The proportional and integral terms are summed to calculate the output of the PI controller. Defining u(t) as controller output, the final form of pi algorithm is,

$$u(t) = MV(t) = Kp\, e(t) + Ki \int_0^t e(t)\, d\tau$$

Where, Kp is the proportional gain, a tuning parameter, Ki is the integral gain, a tuning parameter, t is the time or instantaneous time (the present), τ is the variable of integration (takes on values from time 0 to the present t)Equivalently, the transfer function in the laplace transform of the PI controller is,

$$L(S) = Kp + {}^{Ki}/_{S}$$

Where, s is the complex frequency

The proportional term produces an output value that is proportional to the current error value. The proportional response can be adjusted by multiplying the error by a constant K_p, called the proportional gain constant. The Flow chart diagram of PI controller which consist of a comparator block for comparing the set point and measured value for generating the error signal. The error value obtained which will be valued with the gain and obtained signal which will be a discrete one.

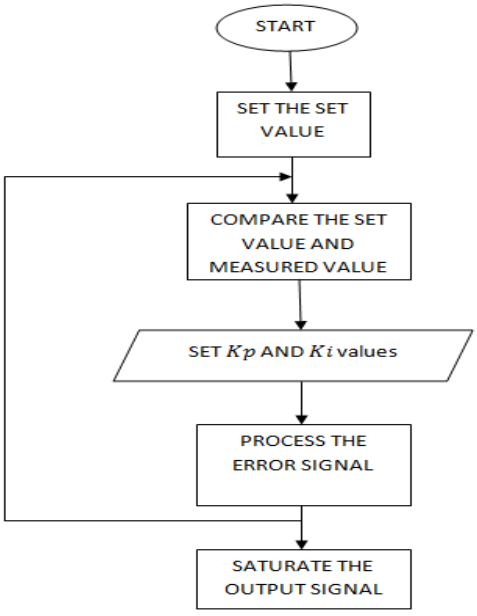

Fig.4. Flow chart of PI Controller

The process block which contains a saturation for limiting the obtained value. By limiting the signal and compared with the reference signal in PWM Generator. The controller output is given by,

$$\mathbf{Kp}\,\Delta + \mathbf{Ki}\int \Delta\ \mathbf{dt}$$

Where, Δ is the error or deviation of actual measured value (***PV***) from the set point (***SP***).

$$\Delta = \mathbf{SP} - \mathbf{PV}$$

$$\mathbf{C} = \frac{\mathbf{G}(\mathbf{1} + \boldsymbol{\tau}\mathbf{s})}{\boldsymbol{\tau}\mathbf{s}}$$

Where, $G = Kp =$ Proportional Gain

$^{G}/_{\tau}$ = Ki =Integral Gain

Setting a value for G is often a trade off between decreasing overshoot and increasing settling time. The lack of derivative action may make the system more steady in the steady state in the case of noisy data. This is because derivative action is more sensitive to higher-frequency terms in the inputs.

2.4 UPFC with SA Algorithm

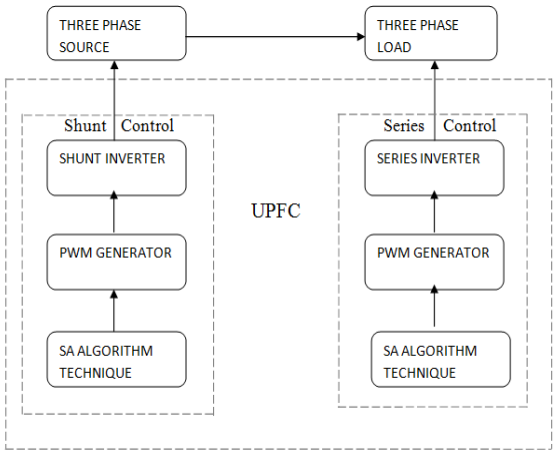

Fig.5. schematic diagram of SA Algorithm

In this system the Simulated Annealing Algorithm is used to compare the voltage and current with real time. So that the triggering signal obtained after the comparison with real time will be efficient one instead of fixed value comparison. After running the values in SA Algorithm the signal generated will be fed to the PWM generator where triggering gate pulse will be generated for switching transistors in Shunt and series component.

III. Simulation Work and Results

3.1 UPFC Using SPWM Method

In this method, the UPFC control signal is directly given by PWM generator. The normal sinusoidal pulse is compared with trigger or triangular signal. The output of the PWM generator is directly given to the UPFC. This method is an open loop function. Because, the PWM signal is directly given to the UPFC and the feedback signal is does not consider. The UPFC always doesn't works on the source side. The UPFC works depends on the balanced sinusoidal wave. In this Simulink diagram, the sine wave and input wave compared which results in production of pulses.

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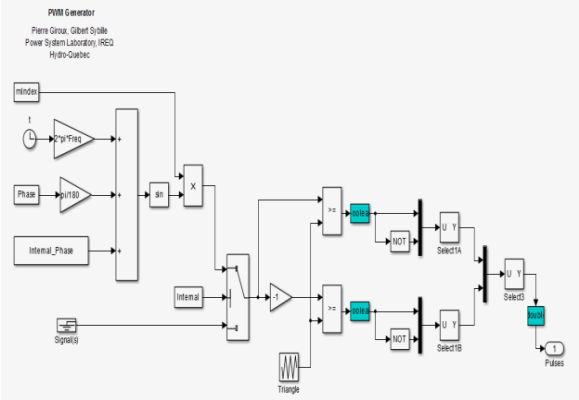

Fig.7. Simulation diagram of PWM generator

The pulse is compared with the triangular wave to obtain the triggering pulse to converter circuit. The pulses used for operating the controller switches in the converter circuit. Accordingly the output harmonics are reduced. The compared signal is converted in to triggering pulse which is applied to gate terminals of shunt and series components. The input of UPFC is taken from 7th bus of the system connected with symmetrical load. That supply and pulses are given to the converter circuit. The switching operation taking place according to pulse signal.

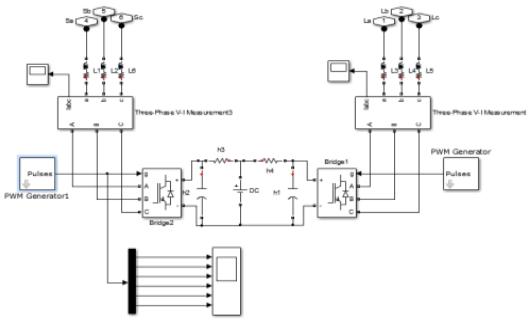

Fig.8.Simulation diagram of UPFC with PWM generator

The output of the UPFC is directly given to 8th bus of the system. The harmonics of input which will be eliminated from the supply power.

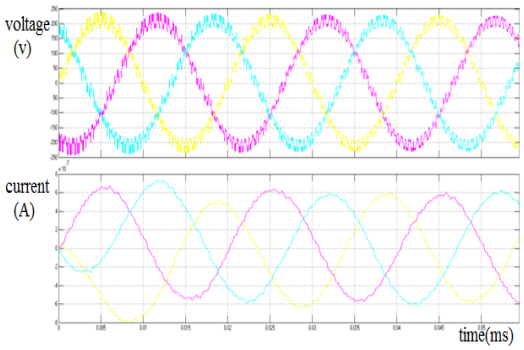

Fig.9.Output waveform of voltage and current in UPFC using SPWM method

This output waveform represents voltage and current signal in which the voltage is maintained < 250 volts even though the input signal is compensated harmonics content are present on it. The current which is maintaining above 6 A which also contains harmonics on it. To reduce total harmonics distortion the method of triggering the converter has to be changed by closed loop or comparing values with real time methods.

The figure represents the Active power, on both real power and reactive power harmonic are present on it.

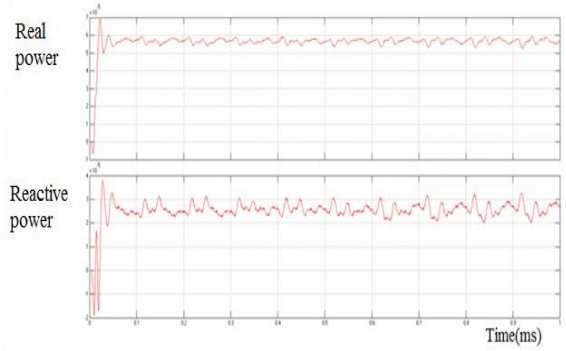

Fig.10.Waveform of Apparent power

The reactive power which reaches the peak of 4 and stacks the value at 3 with slight harmonic distortion.

3.2 UPFC using PI Controller

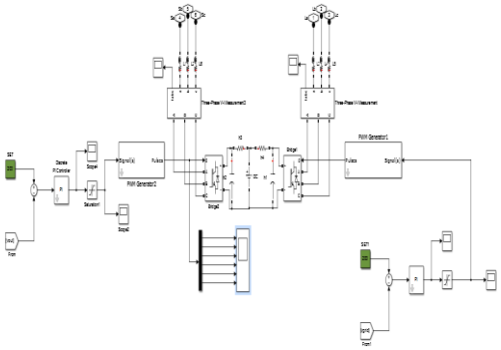

Fig.11. Simulink diagram of PI Controller in UPFC

This is the simulink diagram of upfc contains PI Controller, before an pwm generator. The processing of error signal is going to take part on it. The error signal is going to be generated by comparing the set value (SV) and measured value (PV) by summing block. The generated error will be fed to PI block where the block is set with Kp and Ki values. After the added gain constant with the error signal the output is given to pwm generator. Where the signal is made to compare with triangular pulse and generated pulsating signal is applied to universal bridge circuit. The constant values of Kp and Ki are set with 0.27 and 0.05 according to the error signal generated. The sample time is set with $50e^{-6}$. The PWM pulse generated are fed to the universal bridge block. This process is similar for both series and shunt bridge circuit. Where the shunt controller is connected across the supply side and the series controller is connected across the load side. The both bridge circuit will be doing the same operation but the difference is in the obtained measured value (PV).

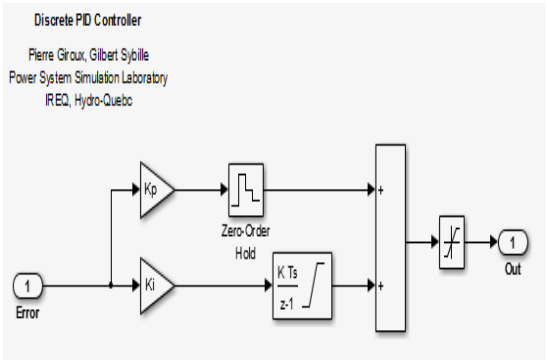

Fig.12. Simulink model of PI controller block

This block in which the error signal Δ is given as input obtained after summing the set value (SV) and measured value (PV). The processing of error signal is done by fixing the Kp and Ki after summing the error by adding gain on to it. The gain constant applied 0.27 and 0.05. The output of the sum which is made to saturate by a 60 before which linearly increasing. The saturated output which is fed to the PWM generator signal. In Fig.13, the sine wave and input wave compared which results in production of pulses. The pulse is compared with the triangular wave to obtain the triggering pulse to converter circuit. The pulses used for operating the controller switches in the converter circuit. Accordingly the output harmonics are reduced.

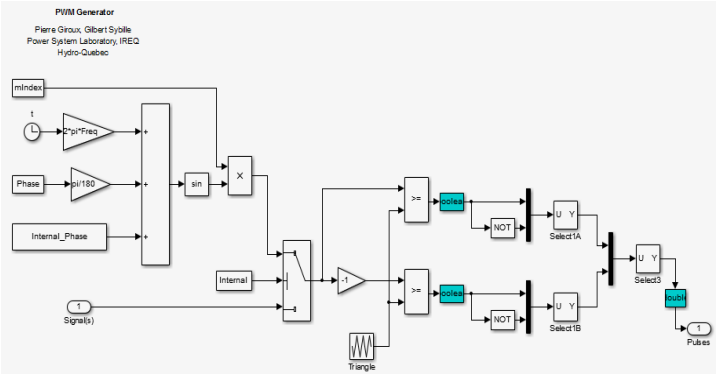

Fig.13. block diagram of PWM generator

The Fig.14, which shows the output waveform of voltage and current after eliminating the distortions on input waveform. The power flow controlled waveform of active and reactive power are shown which is as better compared to SPWM method.

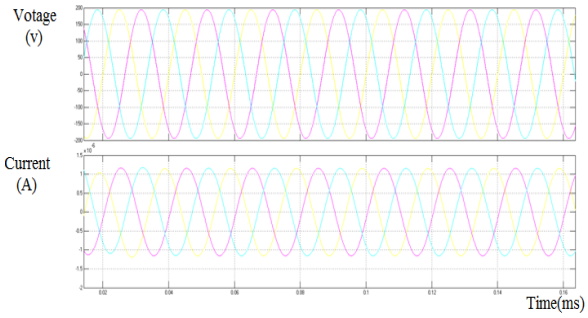

Fig.14. output waveform of PI Controller in UPFC

It is a Output waveform of PI Controller in UPFC connected bus. The voltage is nearly maintained at 200 set value and the current value is maintain at 1.1 mA. The input voltage which contains harmonics due to load. The Fig.15, which represents the compensated real and reactive power using UPFC by PI controller circuit. The obtained real and reactive which is smooth in action and also better than the PWM method which is containing harmonics.

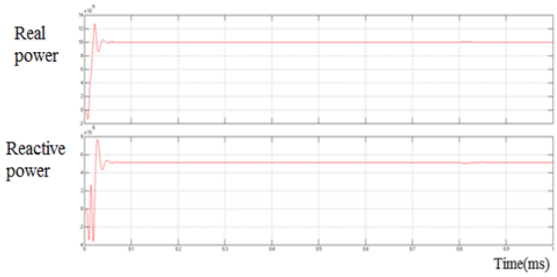

Fig.15. output waveform of apparent power using PI controller in UPFC

Even though a slight oscillations present on it. The reactive power reaches the peak of 8 and settles at constant by 5.

3.3 UPFC using SA Algorithm

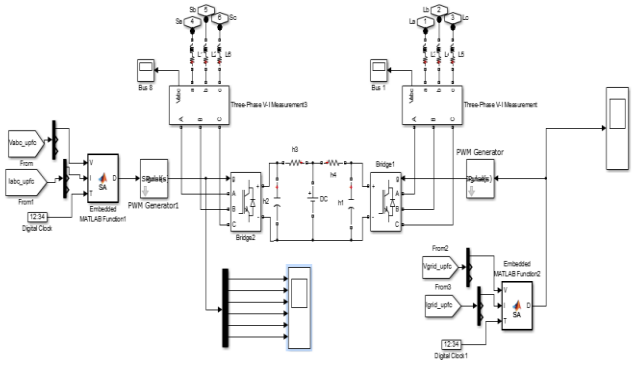

Fig.16. Simulink diagram of UPFC using SA Algorithm

The Simulated Annealing Algorithm, which has been used by running the values of voltage, current and time on the SA Algorithm. The obtained signal after running it is used as import signal and sine signals are compared obtained signal is used for triggering the converter circuits. The Fig.17, which represents the output waveform of voltage after eliminating the distortions on input waveform. The power flow controlled waveform of active and reactive power are shown which is as better compared to SPWM method.

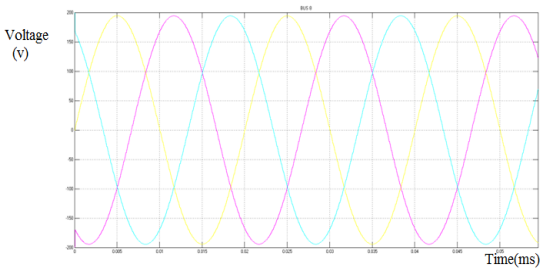

Fig.17. output waveform of voltage in SA Algorithm using UPFC

It is an Output waveform of SA Algorithm in UPFC connected bus. The voltage is exactly maintained at 200 set value. The input voltage which contains harmonics due to load.

The Fig.18, which represents the output waveform of voltage parameter using the SA Algorithm. In this method the power which is compared with real clock so the power factor which contains no distortions in both active and reactive power.

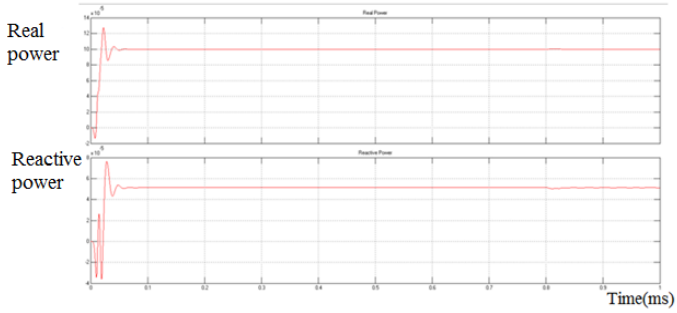

Fig.18. waveform of apparent power in UPFC

The waveform represent active power in that reactive power reaches a peak value of 8 and then stags the value of power at 5 at constant. In this according to the triggering pulse applied to converter circuit.

Parameters	PWM	PI	SA
Voltage	240	190	200
Harmonics reduced	74%	85%	95%

Table.1 Voltage and Harmonics Comparison

IV. Conclusion

The above waveforms are output results of voltage regulation and reactive power compensation of 14 bus power system working with MATLAB SIMLINK model environment. There are three different type of methods used. In this three method SA algorithm is more efficient method. And this method also reduced harmonics and maintain the constant voltage in the bus system.

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