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Implementation of High Speed OFDM Transceiver using FPGA

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Abstract - Proficient, multi mode and re-configurable architecture of interleaver/de-interleaver for multiple standards, like DVB, OFDM and WLAN is presented. Interleaver plays vital role in 4G technologies to recover symbols from burst errors. The aim of our work is to design a reconfigurable modulation technique called Adaptive modulation scheme uses QAM, QPSK and BPSK modulation that adapt themselves based on channel Signal to Noise ratio. Subcarrier allocation algorithm specifically used to focus on utilizing channels with high gains. Our proposed model can achieves a data rate of min 2.5 Gbps as per 3GPP standard by adaptive modulation technique using QAM, BPSK and QPSK.

Key terms: IEEE 802.16e, OFDM, BPSK (Binary Phase Shift Key),QPSK(Quadrature Phase Shift Key),QAM(Quadrature Amplitude Modulation).

INTRODUCTION

OFDM represents an IEEE metropolitan access standard (IEEE 802.16) that provides wireless broadband to fixed CPEs (customer premises equipment) and mobile terminals. The system offers a wide variety of services including voice, data and multimedia. Based on the IEEE 802.16-2004 standard, OFDM allows for an efficient use of bandwidth in a wide frequency range, and can be used as a last mile solution for broadband internet access.

In brief for increasing speed of the OFDM transceiver an address generator for reconfigurable Interleaver/De-interleaver is used. The literatures of the existing papers are explained about certain advantage and disadvantage is used to make new advanced implementation. OFDM physical layer model is increase the performance evaluation. But this model build using MAC PDU by physical layer [1].Using LUT based address generator for Interleaver/De-interleaver is combining the incoming data streams into a block can reduce the continuous memory access [3]. 1/2 code rate based address generator is used for FPGA implementation of the Interleaver of OFDM (IEEE802.16e standard) [4].FSM based same interleaver is used for increasing the speed of the OFDM system. It uses permissible code rates and modulation schemes [5]. 2D realization of the interleaver is used to reduce the memory to achieve hardware efficiency [2].

LUT based technique has the lengthy expression and complicated. Compare to [base paper number] LUT technique is slow in operation and consuming large logic resources [6]. [1] Mathematical algorithm is developed to eliminate the requirement of floor function. It makes the low complexity for FPGA implementation. Mathematical algorithm makes low-complexity architecture for address generator when digital hardware is realize. The block interleaver is make complexity when block size is large. Fixed modulation is used in QPSK, BPSK and QAM.Because of Fixed modulation Speed of the OFDM transceiver will reduce. Interleaver/De-interleaver is not reconfigurable, so process of interleaving/de-interleaving process will take more time. For that proposed hardware architecture is introduced. This architecture is modeled in Verilog and implemented in Altera. The rest of the paper has been organized as follows:

I - System Description
II -Adaptive modulation
III -Interleaver/Deinterleaver Structure
IV -Proposed algorithm
V -Simulation Result
VI –FPGA Implementation Result
VII-conclusion

I- SYSTEM DESCRIPTION

Figure 1 shows block diagram of a simple OFDM System. The transmitter block used Signal generator, Serial to Parallel converter, Convolutional code encoder, convolutional interleaver, adaptive modulator, pilot carrier insertion, inverse FFT (IFFT), and guard interval insertion. The orthogonal frequency division multiplexing (OFDM) is one of the modules in the OFDM system which supports many modulation schemes to implemented by performing FFT and Inverse FFT on the input data stream First data is coming from the signal generator and it will convert serial to parallel using STP converter. Converted input data stream is encoded by Forward error correction coding technique namely convolutional code (CC) encoder. Convolutional interleaver is used to reduce the effect of burst error.

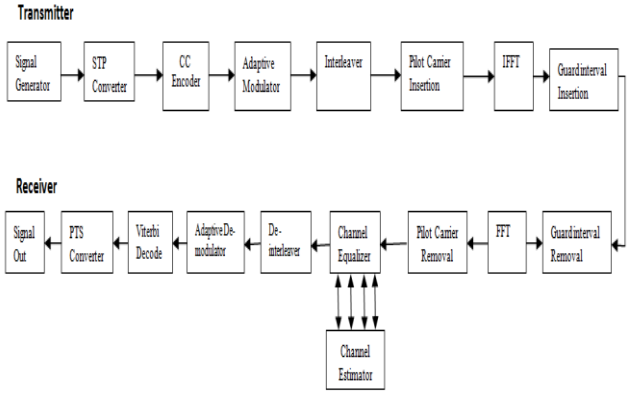

Fig.1. Structure of OFDM Transceiver

Based on channel condition the adaptive modulation permits the wireless system to choose the required higher order modulation. As could increasing the range, can step down to

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lower modulations (in other words, BPSK), but as could are closer to utilize higher order modulations like QAM for increased throughput. The system is capable of reducing the fading and other interference due to Adaptive modulation. In the receiver, the blocks are organized in the reverse order enabling the restoration of the original data sequence at the output.

II -Adaptive modulation

Once the signal has been coded, it enters the modulation block. All wireless communication systems use a modulation scheme to map coded bits to a form that can be effectively transmitted over the communication channel. Representation of complex in-phase and Quadrature-phase (IQ) vector is done by mapping between a subcarrier amplitude and phase to the bits.

Adaptive Modulation and Coding

The specified modulation scheme in the downlink (DL) and uplink (UL) are binary phase Shift keying (BPSK), quaternary PSK (QPSK), 16 Quadrature amplitude modulation (QAM) and 64QAM.To modulate bits to the complex constellation points. For the formation of burst profile FEC options are linked with the modulation schemes. The PHY specifies seven combinations of modulation and coding rate, which can be allocated selectively to each subscriber, in both UL and DL. There are tradeoffs between data rate and robustness, depending on the propagation conditions. Table 1 shows the combination of those modulation and coding rate.

Table 1. Mandatory channel coding per modulation

Modulation	Uncoded Block Size (bytes)	Coded Block Size (bytes)	Overall Coding rate	RS code rate	CC code rate
BPSK	12	24	½	(12,12,0)	1/2
QPSK	24	48	½	(32,24,4)	2/3
QPSK	36	48	¾	(40,36,2)	5/6
16-QAM	48	96	½	(64,48,8)	2/3
16-QAM	72	96	¾	(80,72,4)	5/6
64-QAM	96	144	2/3	(108,96,6)	3/4
64-QAM	108	144	¾	(120,108,6)	5/6

If low SNR, the signal constellation size is reduced in order to improve fidelity, lowering the effective SNR to make transmission more robust. Signal constellation size is improved to allow higher data rate modulation schemes with low probability of error, as a result improving the instantaneous SNR.

III - INTERLEAVER/DEINTERLEAVER STRUCTURE

The convolutional interleaver block permutes the symbols in the input signal. Initially; it uses a set of registers. register length step parameter is depends on the delay value of the kth shift register i.e (k-1) times. The number of shift registers is the value of the row of shift registers parameter.

The block of the Interleaver/Deinterleaver in the OFDM system shown in figure 2.it has the two memory blocks, namely M-1 and M-2 with read/write address generator. In the interleaving block one memory block is beginning to write means another memory block is begin to read and this process will continue vice versa. When sel = 1, write is enabled M-1 is active. During this time period input data stream is written in M-1 means and receives the write address. Simultaneously, input data stream is read from M-2 memory with supplied of read address. After finish the read/write process in memory block upto their desired memory location as specified by interleaver depth, the status of the sel signal is changed the operations.

The block interleaver/Deinterleaver operates with different depths N_{cbps} to various code rates and modulation schemes (table 1) for IEEE 802.16e [7].

Thus,

$$m_k=(N_{cbps}/d).(k\%d)+k/d \quad (1)$$

$$j_k= s.\, m_k/s +(m_k + N_{cbps-\,d.}\, m_k /N_{cbps}) \,\%\, s. \quad (2)$$

Here, $\mathbf{N_{cbps}}$ is the block size corresponding to the number of coded bits per allocated sub-channels per OFDM, d represents number of columns of the block interleaver which is typically chosen to be 16 for OFDM. $\mathbf{m_k}$ is the output after first level of permutation and **k** varies from 0 to N_{cbps} -1. **s** is a parameter defined as $\mathbf{s}= N_{cbpc}/2$, where $\mathbf{N_{cbpc}}$ is the number of coded bits per sub-carrier, i.e., 2, 4 or 6 for QPSK, 16-QAM or 64-QAM respectively.

Table 1.Permitted Interleaver/Deinterleaver Depth in Ieee 802.16e for all Code Rates and Modulation Schemes

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth.Ncbps in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

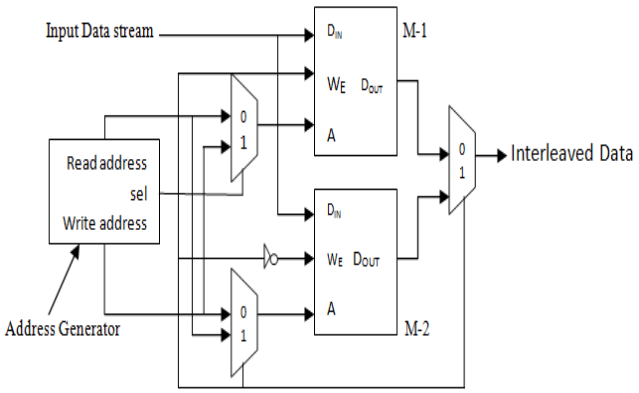

Fig 2. Block diagram of Interleaver/Deinterleaver structure

IV -PROPOSED ALGORITHM

An adaptive modulation scheme is presented for multiuser orthogonal frequency-division multiplexing systems. The aim of the scheme is to minimize the total transmit power with a constraint on the transmission rate for users, assuming

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knowledge of the instantaneous channel gains for all users using a combined bit-loading and subcarrier allocation algorithm. The proposed subcarrier allocation algorithm specifically focuses on utilizing channels with high gains. Thus, in the case of two or more users with higher channel gains than threshold αth, selected by trial and error in a certain subcarrier, the selection of that subcarrier is waived. After the rest of the subcarriers are allocated to the users with the highest gain, the subcarriers are then allocated.

V-SIMULATION RESULT

The proposed hardware of the address generator of reconfigurable Interleaver/Deinterleaver is converted into a Verilog program using Altera. The simulation result is shown in figure 3.In initial process shows the multiple address generation for the Interleaver/Deinterleaver. The adaptive modulation and demodulation is produced the simulation output using all permissible modulation type and code rate adaptively. That the Simulation result is produced using Modelsim-Altera 6.6c (Quartus II).

VI –FPGA IMPLEMENTATION RESULT

Verilog model of OFDM transceiver are implemented and tested into AlteraDE1 FPGA platform. Comparative analysis of the FPGA resource requirement in the delay units of interleaver and Deinterleaver taken together for two implementation. Our proposed implementation technique saves 50% and above 81% of FPGA resources compared to existing implementation. Use of lesser slices leads to reduce the delay in the interconnection network inside the FPGA. The future implies reduction in power consumption too. Due to efficient modeling, the convolutional interleaver, de-interleaver uses very few FPGA resources to be implemented on the same FPGA chip.

VII-CONCLUSION

In this paper design of OFDM transceiver described by Verilog using FPGA and simulated using Modelsim 10.1 and targeted on Altera cyclone II 2c20.The proposed address generator for OFDM reconfigurable interleaver, de-interleaver supporting all possible code rates and modulation patterns as per IEEE802.16e.The proposed algorithm is converted into digital hardware circuit. The hardware is implemented on the Altera DE II FPGA using Verilog.

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