Indian Journal of Emerging Electronics in Computer Communications,
Volume.3, Issue.1, 2016, Page.548-551
www.scientistlink.com/ijeecc

Design of Reversible FFT Algorithm

Dr.M.Saravanan
Professor,
Department of Electronics and Instrumentation Engineering
Sree Vidyanikethan Engineering College, Tirupati, India
mgksaran@yahoo.com

Abstract: *Fast Fourier Transform (FFT) is the most important computation involved in almost all signal processing task, in which, (N/2)log$_2$N umbers of complex multiplications and* ***N log$_2$N*** *numbers of complex additions are involved. Where N is the size of FFT and it is based on the input data length. when the input data length is high, automatically the number of computation of multiplication and addition involved also increases and intern increases the energy consumed by the system. Hence it is emerging fact that the increase in energy consumption must be reduced and which can be easily achieved with the use of reversible logic gates. In the contest of designing reversible logic circuits for FFT implementation become essential. This paper proposes a design of Reversible FFT in both form DIT and DIF using reversible gates.*

Keywords*: Reversible Logic gates, Reversible FFT, Quantum computing, Low power design.*

I. INTRODUCTION

One of the major goals in modern circuit design is reduction of power consumption. As demonstrated by Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Hence, in 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. In most of the signal processing application the primary stage of processing starts with frequency analysis of the incoming signal which was carried out with the application of FFT algorithm, hence it is essential for implementing FFT algorithm using reversible logic gate so that maximum power can be saved. This paper presents design of reversible FFT algorithm implementation.

II. LITERATURE SURVEY

The performance of the reversible circuit based on the following parameters, Garbage outputs, Number of Reversible gates used, Total delay generated by the circuit and number of constant inputs[3]. More specifically the Garbage outputs and Number of reversible gates are the critical parameters in the design. For the best design of reversible circuit the number of garbage and number of gates must be very less. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback [4].Bidet et al. (1995) proposed a first VLSI single chip dedicated for the computation of direct or inverse Fast Fourier transform of up to 8192 complex points. Due to its pipelined architecture it was reported that it can perform 8000 FFT every 400 µs and 1000 FFT every 50µs. In that approach it is mentioned, the design is made such that all the storage is on-chip, so no external memories are required. A new internal result scaling technique, called convergent block floating point, has been introduced in order to minimize the required storage for a given quantization noise[6].

III. PROPOSED REVERSIBLE 2 – POINT DIT-FFT ALGORITHM

The basic structure of 2-Point DIT-FFT algorithm consists of Adders, Subtractor and Multipliers for its functional implementation. For Reversible 2-Point DIT-FFT algorithm implementation the building blocks of the structure should also be reversible, hence first the Adders, Subtractor and Multipliers are implemented with reversible logic gate and the designed Reversible Adder, Reversible Subtractor and Reversible Multipliers are used to construct the Reversible FFT. Apart from these three blocks one more important data needed of the FFT implementation is the Twiddle factor

generator[5]. Even that twiddle factor generator also designed with reversible logic gates, now it's time to design Reversible FFT structure using all the above mentioned reversible blocks. The Figure 3.1 shows the block diagram of Reversible 2-Point DIT-FFT implementation using reversible circuits. In the data entering the FFT unit the A(1) input is fed to reversible multiplier unit and there it is weighted with the Twiddle factor of W_2^0 and then it is sent to next stage were the reversible floating point adder and reversible floating point Subtractor present and accumulate the result from the multiplier and A(0). Since the internal building blocks are reversible the FFT implemented also considered being reversible.

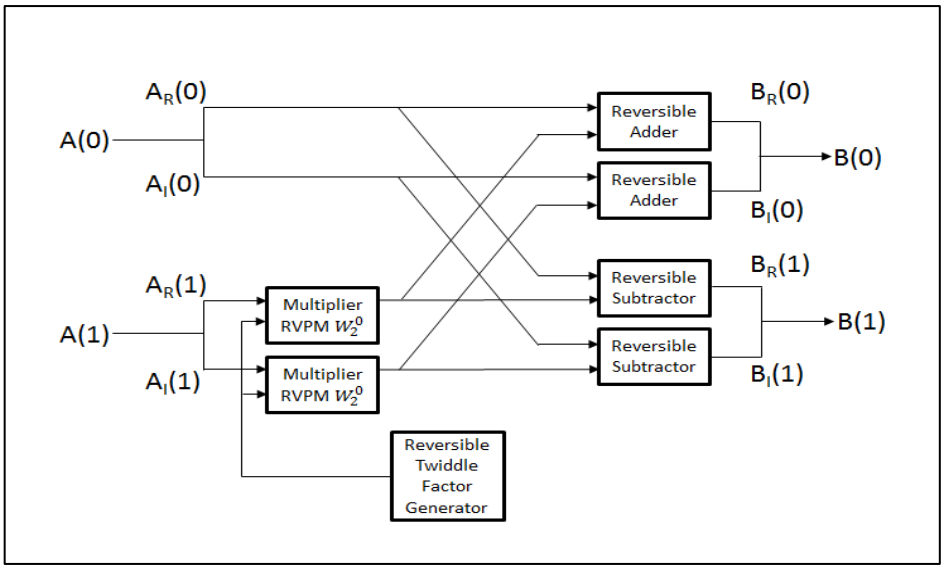
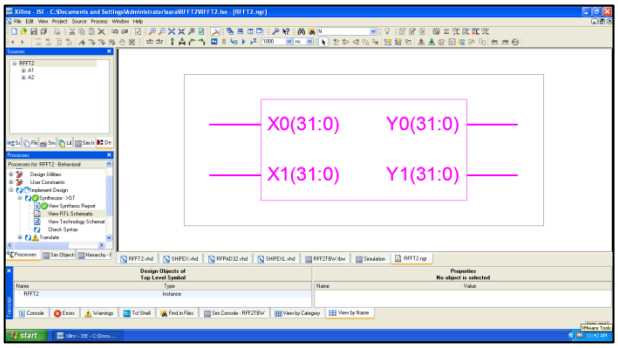


Figure 3.1: Block diagram of 2 Point DIT-FFT algorithm

IV. Radix -2 DIT- FFT IMPLEMENTATION

The proposed Reversible FFT implementation is simulated using Xilinx and results are verified and show in the figures given below.



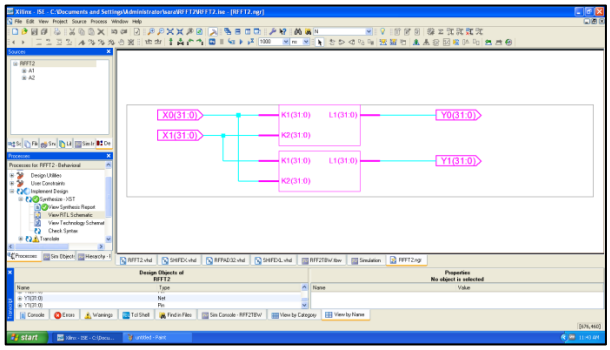


Figure 4.1 Reversible 2-Point Radix-2 DIT-FFT. **Figure 4.2 RTL diagram of Reversible 2-Point Radix-2 DIT FFT**

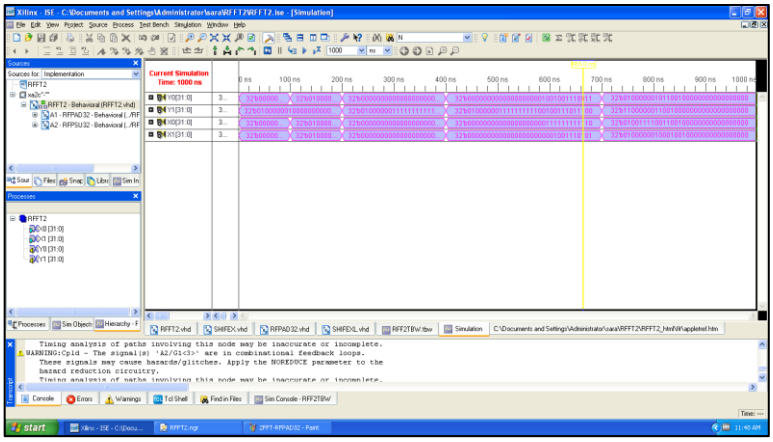


Figure 4.3 Simulation result of Reversible 2-Point Radix-2 DIT FFT

V. CONCLUSION

The paper presented the design of Reversible FFT implementation. In this paper design for 2-Point DIT-FFT algorithm alone discussed and the work may as it is extended for any (N) Point FFT implementation not only that it also possible to implement same for DIF (decimation in Frequency) algorithm. The Speed comparison of FFT implementation is tabulated below.The table show the speed improvement in the proposed reversible FFT implementation of nearly 12 times the conventional approach. The Energy consumption of the proposed design may be calculated when it is implemented using reversible logic gates due to unavailability and unreliability of reversible logic gates the energy improvement was not included in the result may be in the near future once the reversible logic design become physically realizable it is possible to implement energy efficient design of FFT algorithm.

Table 5.1: Comparative study of conventional multiplier and reversible multiplier and speed improvement

Size of FFT (N) - Point	**Using Conventional Multiplier (time delay)**	**Using Reversible Multiplier (time delay)**	**Speed Improvement in FFT implementation using Reversible Logic gate**
2	T_C	$0.083T_C$	12 times
4	$2*T_C$	$0.166\ T_C$	24 times
8	$3*T_C$	$0.249\ T_C$	36 times
16	$4*T_C$	$0.332\ T_C$	48 times
N	$\log_2(N)*\ T_C$	$\log_2(N)\ *\ 0.083$	$\log_2(N)*$ 12 times

REFERENCES

[1]. Landauer, R., 1961. Irreversibility and heat generation in the computing process, IBM J.Research and Development, 5 (3): 183-191.
[2]. Bennett, C.H., 1973. Logical reversibility of computation, IBM J. Research and Development, 17: 525-532.
[3]. Feynman, R., 1985. Quantum mechanical computers, Optics News, 11: 11-20.
[4]. D.M.Smith, 2003. Using Multiple Precision Arithmetic, IEEE Journal of Computing in Science & Engineering .
[5]. Saravanan M, Suresh Manic K, 2013. Novel Reversible Code Converters Using Reversible Logic Gates, International Journal of Electrical and Electronics Engineering Research, Vol. 3, pp.161-166.
[6]. Rohit Sreerama, Paidi Satish, Neelima K, 2012. An Algorithm for Variable Precision Based Floating Point Multiplication, Springer, pp 238-242.