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Optimal Structures for Cascaded Multilevel Inverter

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Abstract-The general function of a multilevel inverter is to synthesize a desired output voltage from several levels of dc voltages as inputs. In order to increase the steps in the output voltage, a new H- bridge topology is recommended which benefits from a series connection of several sub-multilevel inverters. In addition, for producing an output voltage with a constant number of steps, there are different configurations with a different number of components. In this paper, the optimal structures for H- bridge topology are investigated for various objectives such as minimum number of switches and dc voltage sources and minimum standing voltage on the switches for producing the maximum output voltage steps. Two new algorithms for determining the dc voltage sources magnitudes have been proposed. Finally, in order to verify the theoretical issues, simulation results for 25 level inverter with a maximum output voltage of 120V are presented.

I. INTRODUCTION

The concept of utilizing multiple small voltage levels to perform power conversion was carried over thirty years ago [1- 3]. The advantages include enriched power quality, less electro-magnetic compatibility, low switching losses and high voltage blocking capability [4]. Three bench mark topologies namely cascaded diode clamped and flying capacitor multilevel inverter have been came into existence in the past four decades [12]. Baker *et al* patented the cascaded H-bridge and diode clamped structures in 1975 and 1980. It utilizes isolated dc sources or a bank of series capacitors to split the dc bus voltage to create higher power quality [3] [5]. In Mixed-level hybrid multilevel cells [13], the H-bridge cells of the cascaded leg are substituted with diode-clamped or flying-capacitors[6]. To reduce the number of separate dc sources for high-voltage high-power applications, new configurations have also been presented [14] [15]. Recently, several multilevel converter topologies have been developed [18][20]. The cascaded H-bridge inverter is a very modular solution based on a widely commercialized product [7] [26]. This has a good effect on the reliability and maintenance of the system since the cells have high availability, intrinsic reliability and a relatively low cost. Unfortunately, the inverters do have some disadvantages [16]. One particular disadvantage is the greater number of power semiconductor switches needed. Although, lower voltage rated switches can be utilized in a cascaded multilevel converter, each switch requires a related gate driver and protection circuits [24]. This may cause the overall system to be more expensive and complex. The topology consists of series connected sub-multilevel inverter blocks using H-Bridge Inverters [8]. In this topology, the modulation strategies and the structures of the different cells and the required switches are the same [10]. Thus, in order to reduce the cost of the inverter, it is necessary to introduce an optimal structure with the minimum number of components. In this paper, in order to generate all the steps (odd and even) at the output voltage, two new procedures for calculating the magnitudes of the required dc voltage sources are proposed [9]. In addition, this paper proposes an optimal structure for this type of multilevel converter with a high number of steps associated with a low number of power switches and dc voltage sources [25]. This results in a reduction in cost for the converter [11]. Finally, this paper includes a design example of a multilevel inverter.

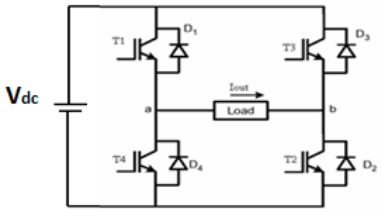

Fig .1 single phase full bridge inverter

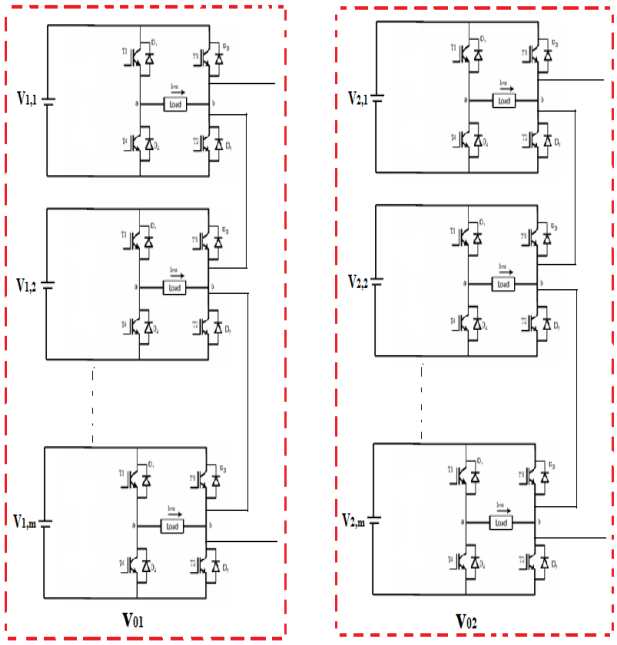

Fig. 2 Cascaded sub-multilevel inverter

II. CASCADED H BRIDGE INVERTER

The basic unit for the multilevel inverter showing in Fig .1 consists of a dc voltage source (with a voltage equal to V_{dc}) with four unidirectional switches. It is noted that three levels can be achieved for V_o using the basic unit shown in Fig. 1 and

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it can be extended as sub-multilevel structure is also illustrated in Fig. 2. The basic units in series can increase the possible values of V_o. If *n* dc voltage sources are used in the extended with *k* basic units in series as shown in Fig. 2, then the number of output voltage steps (N_{step}) and switches (N_{switch}) are given by the following equations, respectively:

$$N_{step} = n(n+1)+1 \quad (1)$$

$$N_{switch} = 4(n+1) \quad (2)$$

$$N_{step} = \prod_{i=1}^{k}[n_i(n_i+1)+1] \quad (3)$$

$$N_{switch} = \sum_{i=1}^{k}[2(n_i+1)] \quad (4)$$

$$v_0(t) = \sum_{j=1}^{k} v_0, j \quad (5)$$

$$v_o, \max = \sum_{j=1}^{k}\sum_{i=1}^{n_j} v_i j \quad (6)$$

III. PROPOSED ALGORITHIMS FOR THE DETERMINATION OF MAGNITUDES OF dc VOLTAGE SOURCES

As mentioned previously, to determine the values of the dc voltage sources, an algorithm is required to utilize a lower number of dc voltage sources and power switches.

A. First Proposed Algorithm

In this algorithm, it is proposed that the values for all of the dc voltage sources for generating odd and even steps can be calculated using the following relationships:

First stage:

$$v_{1,1} = v_{dc} \quad (7)$$

$$v_{j,1} = 2v_{dc} \quad j=1, 2, 3,\ldots\ldots\ldots\ldots\ldots..,n_1 \quad (8)$$

Second stage:

$$v_{1,2} = v_{dc} + 2\sum_{j=1}^{n_1} v_{j,1} = (4n_1 - 1)v_{dc} \quad (9)$$

$$v_{j,2} = 2(4n_1 - 1)v_{dc} \quad j=1, 2, 3,\ldots\ldots\ldots\ldots..,n_2 \quad (10)$$

m^{th} stage:

$$v_{1,m} = v_{dc} + 2(\sum_{j=1}^{m-1}\sum_{l=1}^{n_j} v_{j,1}) \quad (11)$$

$$v_{j,m} = 2v_{1,m} \quad (12)$$

B. Second Proposed Algorithm

For a greater reduction in the variety of the values of the dc voltage sources, another new algorithm is proposed as follows:

$$N_{step} = \prod_{i=1}^{k}(4n_i - 1) \quad (13)$$

First stage:

$$v_{j,1} = v_{dc} \quad j=1, 2, 3,\ldots\ldots\ldots\ldots\ldots..,n_1 \quad (14)$$

Second Stage:

$$v_{j,2} = v_{dc} + 2\sum_{i=1}^{n_1} v_{i,1} = (2n_1 - 1)v_{dc}$$

$$j=1, 2, 3,\ldots\ldots\ldots\ldots\ldots..,n_2 \quad (15)$$

m^{th} Stage:

$$v_{j,m} = v_{dc} + 2(\sum_{j=1}^{m-1}\sum_{l=1}^{n_j} v_{j,1}) \quad (16)$$

Let the position of cell be *l*, the total number of dc sources in cell be n_i and the total number of stages be *m*.

$$N_{step} = \prod_{i=1}^{k}(2n_i + 1) \quad (17)$$

IV. OPTIMAL STRUCTURES BASED ON THE TOPOLOGY PROPOSED

For a constant number of dc voltage sources and their possible arrangements in different stages, it is possible to obtain a different number of steps at the output voltage utilizing a different number of power switches [17]. For example with four dc voltage sources and 16 power switches, if there are two dc voltage sources in the first stage and one in the second stage, the number of steps at the output will be 15. While using two dc voltage sources in each stage and utilizing the same number of power switches the output steps will be equal to 25 [19]. By utilizing more dc voltage sources, the repetition of such states will grow [21]. There is a great variety of configurations for a constant number of dc voltage sources. Therefore, to choose the optimal structure for a special state because this ability leads to a reduction in the size, weight and cost of the converter [22]. Considering the great variety of existing configurations, the optimal structures are proposed in the following sections.

a. Optimal Structure for the Minimum Number of Switches with a Constant Number of dc Voltage Sources

The question concerning the proposed structure is that if the number of dc voltage sources ($N_{capacitor}$) is constant, which topology can provide a minimum number of switches (N_{switch}). Suppose the converter consists of a series of *k* stages each with n_i dc voltage sources (i = 1, 2,……., *k*). Thus

$$N_{capacitor} = n_1 + n_2 + n_3 \ldots\ldots + n_m = cte \quad (18)$$

Considering (6), the number of switches is given in (7),

$$N_{switch} = [2(n_1+1)]+[2(n_2+1)]+[2(n_m+1)] \quad (19)$$

b. Optimal structures for a minimum number of switches with a constant number of voltage steps

The objective of a multilevel converter is to obtain the maximum step number with a minimum of switches. The question concerning the proposed structure is that if the number of voltage steps (N_{step}) is constant, which topology can provide a minimum number of switches.

The number of levels and switches can be represented as

No of levels $= 2n+1$

No of switches $= 4n$

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Suppose a converter consists of a series of m stages each with n_i (i = 1, 2, …… ,*m*) dc voltage sources as shown in Fig. 2. The number of switches is given by (9). Considering, the number of output steps is given as follows:

$$N_{step} = \sum_{j=1}^{m} [n_j (n_j + 1) + 1] = cte \quad (20)$$

Using the method of the lagrange multipliers, such problems can be solved. For this method, the cost function is defined as follows

$$f = N_{switch} + \lambda g \quad (21)$$

In the above equation, λ is the lagrange multiplier and the function g is as follows

$$g = N_{step} - cte = 0 \quad (22)$$

According to the method of the lagrange multipliers, the minimum number of switches can be calculated by solving the following equations

$$\frac{\partial f}{\partial n_i} = \frac{\partial N_{switch}}{\partial n_i} + \lambda \frac{\partial g}{\partial n_i} = 0 \quad (23)$$

$$\frac{\partial f}{\partial \lambda} = g = 0 \quad (24)$$

The above equations can be rewritten as follows

$$\frac{\partial f}{\partial n_1} = 4 + \lambda\{[2(2n_2+1)(2n_3+1)...(2n_m+1)] - x\}$$

$$\frac{\partial f}{\partial n_2} = 4 + \lambda\{[2(2n_2+1)(2n_3+1)...(2n_m+1)] - x\}$$

$$\frac{\partial f}{\partial n_m} = 4 + \lambda\{[2(2n_1+1)(2n_2+1)(2n_3+1)...(2n_m+1)] - x\}$$

$$\frac{\partial f}{\partial \lambda} = [2(2n_1+1)(2n_2+1)(2n_3+1)...(2n_m+1)] - x = 0$$

$$2n_1 + 1 = s_1; 2n_2 + 1 = s_2; 2n_m + 1 = s_m$$

$$s_1, s_2, s_3 ..... s_m - x = 0$$

Notice that n_j (j = 1, 2, ……, *k*) is an integer and thus S_j is an integer too. If n_j is substituted by an integer between zero and infinity, the answer-set for S_j will be

$$s_j = \{1,3,5,7,.....\infty\} \quad (25)$$

Considering the above answer-set for S_j is obtained as follows

$$s_1 = s_2 = s_3 = ...s_m = s \quad (26)$$

From equation (19), it is obvious that

$$n_1 = n_2 = n_3 = ...n_m = n \quad (27)$$

The above equation denotes that in order to use the minimum number of switches for producing the maximum number of voltage steps, the number of switches must be the same in all stages. Substituting (18) into (5) and (8) results in

$$N_{switch} = 2k(n+1) \quad (28)$$

$$N_{step} = [n(n+1)+1]^k \quad (29)$$

The above equations can be written as

$$k = \frac{\ln N_{step}}{\ln[n(n+1)+1]} \quad (30)$$

Therefore the minimum number of switches will be

$$N_{switch} = \frac{2(n+1)}{\ln[n(n+1)+1]} \ln N_{step} \quad (31)$$

Since N_{step} is constant, N_{switch} will be minimized when 2(*n*+1) = ln [*n* (*n*+1) +1] tends to the minimum.

c. Optimal structure for the minimum number of dc voltage sources with a constant number of voltage steps

The next question is that if N_{step} is the number of voltage steps considered for voltage V_o, which topology with a minimum number of dc voltage sources can satisfy this need.

Suppose the converter consists of a series of 'k' stages each with n_i (i = 1, 2, …….,*m*) dc voltage sources. The number of output voltage steps is given by (10) and the number of dc voltage sources is given as follows

$$N_{capacitor} = n_1 + n_2 + ... + n_m \quad (32)$$

Using the method of the lagrange multiplier the optimal answer is obtained by solving the following equation

$$\sqrt{4s_j} - 3 = s_j \quad (33)$$

$$s_j = 3 \; for j = 1,2,.....m \quad (34)$$

$$n_1 = n_2 = n_3 = ... = n_m \quad (35)$$

The second method for proving the above conclusion is as follows. It can be proven that the minimum number of dc voltage sources may be obtained for an equal number of dc voltage sources in each stage. The number of dc voltage sources is given by

$$N_{capacitor} = n * k \quad (36)$$

$$N_{capacitor} = \frac{n}{\ln[n(n+1)+1]} \ln N_{step} \quad (37)$$

Since N_{step} is constant, $N_{capacitor}$ will be minimized when n= ln [2n + 1] tends to minimum. Where n = 1 gives the minimum number of dc voltage sources to realize N_{step} values for the voltage.

d. Optimal structures for the minimum standing voltage of switches with constant number of voltage steps

The voltage and current ratings of the switches in a multilevel converter play important role in the cost and realization of the multilevel converter. In all topologies, the currents of all the switches are equal to the rated current of the load. However, this is, not true for the voltage. The question is that if N_{step} voltages are considered for V_o, which topology uses the switches with the minimum voltage. Suppose that the peak voltage of the switches is represented by:

$$v_{switch} = \sum_{j=1}^{k} v_{stage,j} \quad (38)$$

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In the above equation, V_{stage}; j represents the peak voltage of the switches in stage $_j$. Therefore, it can be considered as a criterion for the comparison of different topologies from the maximum voltage on the switches. A lower criterion indicates that a smaller voltage is applied at the terminal of the switches in the topology, which is considered an advantage. With reference to the following equations can be obtained.

The maximum standing voltage $s_{1,1}(v_{s1,1})$ is follow

$$v_{s1,1} = v_{1,1} + v_{2,1} + v_{3,1} + \ldots\ldots\ldots + v_{n,1} \quad (39)$$

$$v_{s1,1} = (2^n - 1)v_{dc} \quad (40)$$

The maximum standing voltage $s_{3,1}(v_{s3,1})$ is as follows

$$v_{s3,1} = v_{2,1} + v_{3,1} + \ldots\ldots\ldots + v_{n,1} \quad (41)$$

$$v_{s(2n+1),1} = v_{1,1} + v_{2,1} + v_{3,1} + \ldots\ldots\ldots + v_{n,1} \quad (42)$$

Thus the maximum standing voltage on the switches in the first stage is calculated as follows

$$v_{stage,1} = 2(v_{s1,1} + v_{s3,1} + v_{s(2n-1),1} + v_{s(2n+1),1}) = 2^{n+1}.nv_{dc} \quad (43)$$

The maximum standing voltage on the switches can be obtained as

$$v_{switch} = (n2^{n+1})[v_{1,1} + v_{2,1} + v_{3,1} + \ldots\ldots\ldots\ldots + v_{1,k}] \quad (44)$$

$$v_{switch} = (n2^{n+1})[1 + x + x^2 + \ldots\ldots\ldots\ldots + x^{k-1}]v_{dc} \quad (45)$$

$$x = 2^{n+1} - 1 \quad (46)$$

When

$$v_{switch} = (n2^{n+1})(\frac{x^k - 1}{x - 1})v_{dc} \quad (47)$$

$$v_{switch} = (n.2^n)\frac{(2^{n+1} - 1)(\frac{\ln N_{step}}{\ln[n(n+1)+1]}) - 1}{2^n - 1}v_{dc} \quad (48)$$

VI. SIMULATION RESULTS

To show the performance of the multilevel inverter, using proposed algorithm, the multilevel inverter shown in Fig.2 is simulated using MATLAB R2010b. Several modulation strategies have been reported for multilevel Inverters [23–27]. In this paper, the multicarrier PWM (MCPWM) switching technique is employed to verify the feasibility of the proposed optimal structures for the topology depicted in Fig. 2. For simulation analysis, 2 cells per stage and 2 stages are chosen. The input cell voltages have been calculated using the proposed optimal structures are $V_{1,1}$= $V_{2,1}$=10V and $V_{1,2}$= $V_{2,2}$=50V and R-L load (R = 100 and L = 55mH). Fig. 3 shows the simulation results for the output voltage and current for 25 level respectively. Therefore, the amplitude of the output voltage is found to be 84.27V. The amplitude of the output current obtained from simulation is 1A. The THDs of the output voltage and current based on the simulation are 4.18% and 2.55%, respectively.

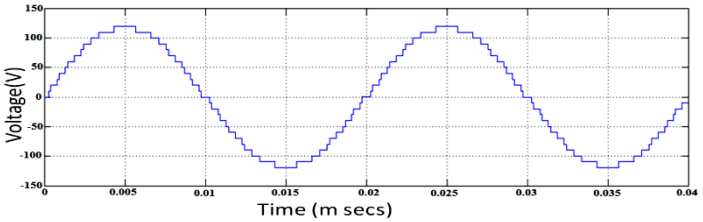
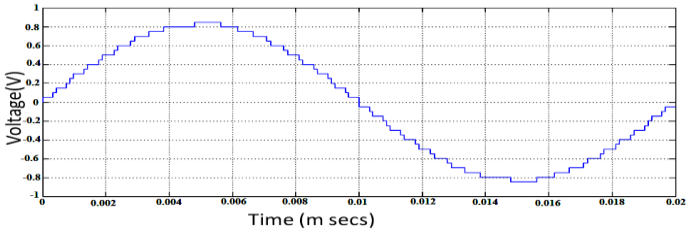
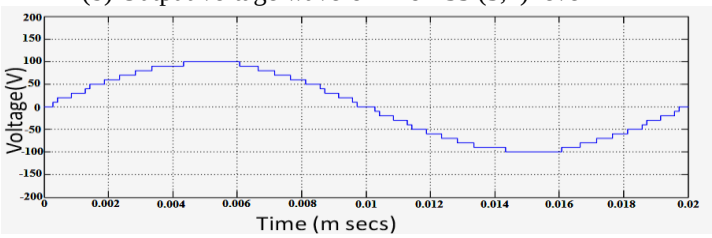


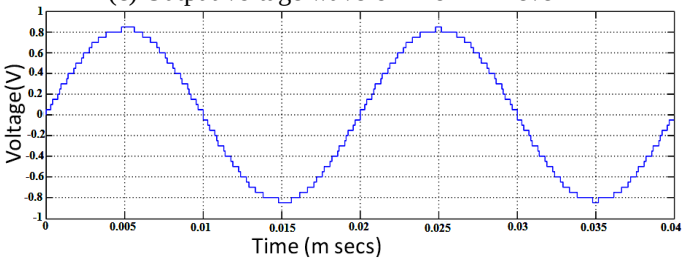
Fig. 3 (a) Output voltage waveform for 25 level



(b) Output voltage waveform for 35 (3,2) level



(c) Output voltage waveform for 21 level



(d) Output voltage waveform for 35 (2,3) level

VIII. CONCLUSION

In this paper, two new algorithms for the determination of the magnitudes of dc voltage sources have been proposed for the cascaded H-bridge topology. It was shown that the structure consisting of units with two dc voltage sources is the best case to keep the minimum number of switches for a certain number of voltage steps.

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