Low Power Design of Johnson Counter Using DDFF Featuring Dual Mode Logic

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Abstract— Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. A new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF are introduced here. Both of them eliminate the drawbacks of existing high performance flip-flop designs. The proposed design mainly reduces the power consumption by eliminating the large capacitance present in the pre-charge node of several existing flip-flop designs by separately driving the output pull-up and pull-down transistors by following split dynamic node structure. This reduces the power up to 40% compared to conventional architectures of flip-flops. The DDFF and DDFF-ELM are compared with other state of the art designs by implementing a Johnson up-down counter. The DML is introduced in Johnson counter improve the speed performance by allowing the system to switch between static and dynamic modes of operation according to its requirements.

Index Terms— *VLSI, flip flops, power dissipation, split dynamic nodes, DDFF-ELM, DML*

I. INTRODUCTION

Over the past decade, power consumption of VLSI chips has been continuously increasing. The need for low-power design is becoming a vital parameter in high-performance digital systems. There are numerous techniques being encountered for the design of low power VLSI circuits. Low power has made an important note that power dissipation has a consideration on performance and area. Static power and Dynamic power being the main components determining the power consumption in CMOS circuits[6]. In synchronous systems, high speed has been obtained using advanced pipelining techniques. In modern pipelined architectures, high speed demands a lower pipeline overhead. The overhead is the latency related with the pipeline elements, such as the flip-flops and latches. The design methodology and area and timing requirements determine the choice of latches and flip-flops[8]. Latches and flip-flips can be static or dynamic. A dynamic latch or flip-flop loses its content as time increases, while a static one retains its content regardless of elapse time. In the past few decades, lot of work has been done to improve the performance of the flip-flops. The flip-flops considered for analysis are PowerPC 603, Hybrid-Latch flip-flop (HLFF), Semi-dynamic flip-flop (SDFF), Conditional pre charge flip-flop (CPFF),conditional data mapping flip-flop (CDMFF) and Cross charge control flip-flop (XCFF). The main trade-offs of any flip-flop are very important for a design engineer when designing a circuit or for a tool that automates the process of design.

Motivation of the Work

The DDFF offers a power reduction of up to 37% and 30% compared to the conventional flip-flops at 25% and 50% data activities, respectively. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons made in a 90 nm UMC process show a power reduction of 27% compared to the Semi dynamic flip-flop, with no degradation in speed performance. The leakage power and process-voltage-temperature variations of various designs are studied in detail and are compared with the proposed designs. Also, DDFF and DDFF-ELM are compared with other state-of-the-art designs by implementing a 4-b synchronous counter and a 4-b Johnson up-down counter. The performance improvements indicate that the proposed designs are well suited for modern high-performance designs where power dissipation and latching overhead are of major concern.

II. RELATED WORK

A. Design of Conditional Data Mapping Flip-Flop For Low Power Applications

The Low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits [3][12]. Our experimental results enabled us to identify the power and performance trade-offs of the flip-flop design. Drawbacks in this design are, 1) In a nano scale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point. 2) Finally it is difficult to apply the low power techniques introduced in previous section to CDMFF.

B. Hybrid Latch Flip-Flop with Improved Power Efficiency

The conditional keeper structure was proposed that avoids clash at the output, saving the power consumed and reducing the delay in the critical path. In addition, another structure is proposed for use in the condition of high activity of flip-flop input[5][11]. The cost for the use of this circuit is somewhat higher power dissipation in regular low-activity input behavior. This design has following drawbacks. In order to change the state of HLFF, the keeper has to be overpowered, which introduces another portion of unnecessary power consumption and increase in the delay.

This is particularly true for the keeper at the output since in some cases, such as pass-transistor logic driven by flip-flop, it has to have certain minimal driving capability, which is the requirement in conflict with the claimed keeper weakness. These disadvantages make HLFF not suitable for applications where low power is required since its power consumption limits its utilization. It is noticed that considerable portion of power dissipated in HLFF occurs due to these unnecessary and false transitions that result in glitches generally increasing the power consumed by consecutive logic as well.

Drawback of this circuit is somewhat higher power dissipation at the low input switching activity (due to the additional circuitry and the load on the internal signal). Also, since the internal node is locked at the high level after one high-to-low and consecutive low-to-high transition of the input, while the output is high, behavior similar to HLFF with respect to previously described glitch at the output can be observed in this particular case.

C. Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic

This paper describes it family of semi-dynamic and dynamic edge-triggered flip-flop which are part of the UtraSPARC-111 microprocessor. They provide short latency, reduced clock load, a good interface to static and dynamic logic, and can easily incorporate logic functions with minimum delay penalty [15], eliminating one gate delay from a critical path. These flip-flops have played an integral role in meeting the Ultra SPARC-III cycle time goal. This design uses conditional shutoff mechanism. It needs larger clock load and larger precharge capacitance. Hence, It consumes high power.

D. Power pc 603 Flip-Flop

Power PC means Performance Optimization with Enhanced RISC Performance Computing. This paper describes the power dissipation is low and also having low clock-to output (CLK-Q) delay. It is one of the fastest classical structures and its main advantage is the short direct path and low power feedback[14].But The large load on the clock will greatly affect the total power consumption of the Flip-Flop. It does have a worse data-to-output latency because of the positive setup time and its sensitivity to clock signal slopes and data feed through is another concern when using it. The large D-Q delay resulting from the positive setup time is one of the disadvantages of this design.

III. PROPOSED SYSTEM

A. DUAL DYNAMIC HYBRID FLIP FLOP

*T*he DDFF possess a hybrid architecture that combines the merits of dynamic and static structures. The performance of modern high performance flip-flops are compared with that of DDFF at different data activity. Dual Dynamic Hybrid Flip-Flop (DDFF) which has additional inv4 involves an extra territory to flip flop and after that its obliges more power. QB in the output is inverted by INV3, gets output as Q. So the output Q is again inverted and it's not needed. A standout amongst the most downside of DDFF is huge area and more power.
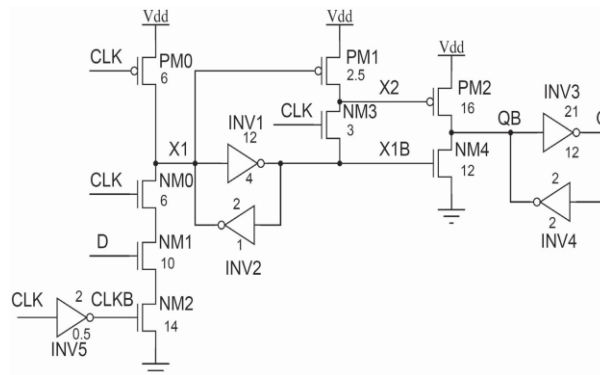
Figure 1: Block diagram of proposed DDFF

The Dual dynamic node hybrid flip-flop (DDFF) eliminates the large pre charge capacitance present in the output node of several conventional designs by following a split dynamic node structure to separately drive the output pull up and pull down transistors. Fig.1 shows the architecture of DDFF. In the DDFF architecture, Node X1 is pseudo-dynamic, with a Weak inverter going about as a keeper, whereas, contrasted with the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is given at the frontend rather than the conditional one in XCFF.

The operation of the flip-flop could be partitioned into two stages:

      1) The evaluation stage, when CLK is high, and
      2) The pre charge stage, at the point when CLK is low.

The genuine latching happens amid the 1–1 overlap of CLK and CLKB amid the evaluation stage. On the off chance that D is high preceding this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 bringing about node X1B to go high and output QB to discharge through NM4. The low level at the node X1 is held by the inverter pair INV1-2 for whatever is left of the evaluation stage where no latching happens.
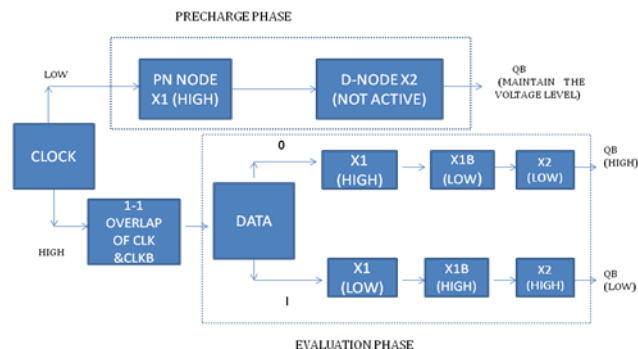

Figure 2: Functional block diagram of DDFF design

Accordingly, node X2 is held high all through the evaluation period by the PMOS transistor PM1. As the CLK falls low, the circuit enters the pre charge stage and node X1 is pulled high through PM0, witching the state of INV1-2. Amid this period node X2 is not energetically driven by any transistor, it stores the charge dynamically. The outputs at node QB and keep up their voltage levels through INV3-4. In the event that D is zero preceding the overlap period, node X1 stays high and node X2 is pulled low through NM3 as the CLK goes high. Along these lines, node QB is charged high through PM2 AND NM4 is held off. At the end of the evaluation stage, as the CLK falls low, node X1 stays high and X2 stores the charge dynamically.

The architecture shows negative setup time since the short transparency period characterized by the 1–1 overlap CLK of and CLKB permits the information to be sampled significantly after the rising edge of the CLK before CLKB falls low. Node $X1$ experiences charge sharing when the CLK makes a low to high transition while D is held low. These results in a transient fall in voltage at node $X1$, yet the inverter pair INV1-2 is skewed legitimately such that it has a switching limit well beneath the most detrimental possibility voltage drop at node $X1$ because of charge sharing.

Timing Diagram Of A Flip-Flop

The timing graph demonstrates that Node $X1$ undergoes charge sharing when the CLK makes a low to high transition while D is held low. This result in a momentary fall in voltage at node $X1$, but the inverter pair INV1-2 is skewed properly such that it has a switching threshold well below the worst case voltage drop at node $X1$ due to charge sharing. The timing diagram shows that node $X2$ retains the charge level during the pre charge phase when it is not driven by any transistor. Note that the temporary pull down at node $X2$ when sampling a "one" is due to the delay between $X1$ and $X1B$.
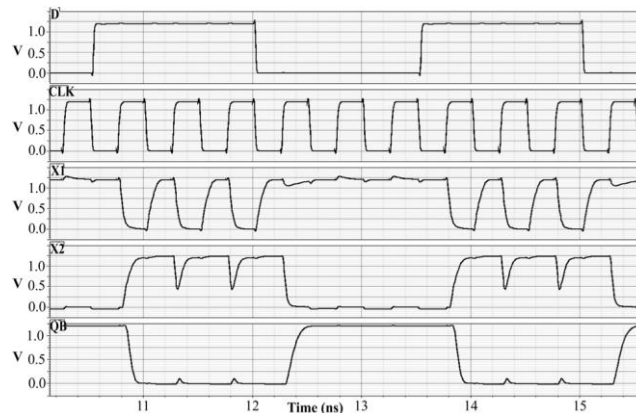

Figure 3: Timing diagram of DDFF

The above figure shows the post-layout timing diagram of the flip-flop at 2-GHz CLK frequency and 1.2 V supply in 90-nm UMC (United Microelectronics Corporation process technology)

Setup Time and Hold Time of A Flip-Flop

The setup time and hold time of a flip-flop refers to the minimum time period before and after the CLK edge, respectively where the data should be stable so that proper sampling is possible. Here setup time and the hold time depend on the CLK overlap period. If VM is the switching threshold of the inverter pair INV1-2 and Tvm is the time required to discharge node $X1$ to VM, the hold time required by the flip flop can be expressed as;

$$T\text{hold1} \geq T\text{vm} \quad (1)$$
$$T\text{hold0} \geq T\text{ov} - T\text{vm} \quad (2)$$

where Tov is the overlap period defined by the low to high transition of the CLK and high to low transition of CLKB. It should be greater than Tvm for the proper functioning of the flip-flop Thold1 and Thold0 represent the hold-time required for sampling a one and a zero, respectively. Also note that Thold1 and Thold0, respectively are the maximum time period after the CLK transition such that the flip-flop samples a zero and a one, respectively.

Since CLKB is high prior to the low to high transition of the CLK, when D is high, the parasitic diffusion capacitors at the drain of $NM1$ and $NM2$ are pre discharged, resulting in a low Tvm. Now the overlap period can be chosen such that Thold1 and Thold0 in (1) and (2), respectively, are minimized. Tov can be adjusted by setting proper size for the transistors in INV5 as specified in [5]. This leads to a small negative setup time and a positive hold time close to zero.
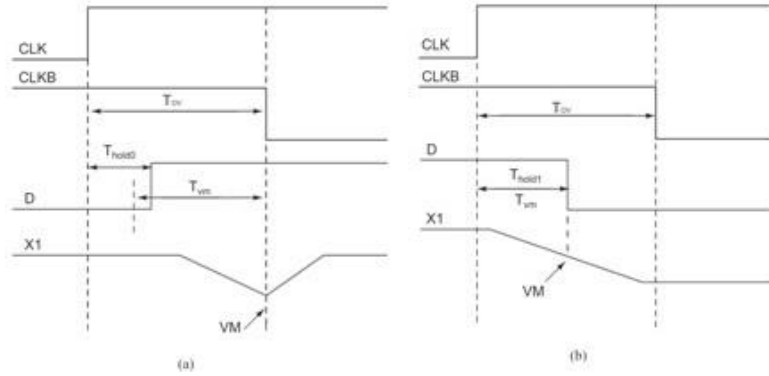

Figure 4: Setup Time and Hold Time

Fig. 4(a)shows hold time for sampling "zero," where D is held low for time-period slightly greater than Tov − Tvm after the positive CLK edge. This causes node $X1$ to discharge to a voltage greater than VM and INV1-2 restores the high level leading to a proper latching of "zero."

A similar case for sampling "one" is shown in Fig. 4(b). Here, since D is held high for a time-period equal to Tvm, node $X1$ properly discharges and "one" is latched. We measured Tvm to be 18 ps in the pre-layout analysis, where only the frontend of the flip flop was simulated with proper load, and an overlap period of 50 ps was chosen. The pre-layout simulation of the flip-flop at 27 °C and 1.2 V supply voltage measures Thold0 to be 30 ps and Thold1 to be 15 ps. The slight variation of the results from that of (1) and (2) is due to the nonzero slopes of CLK and data signals.

B. DDFF-ELM

Dual dynamic node hybrid flip-flop with embedding logic ability (DDFF-ELM) transistor driven by the information data is supplanted by the PDN and the clocking plan in the frontend is changed. The purpose behind this in timing is the charge sharing, which gets to be wild as the number of NMOS transistors in the stack builds. The same reason makes XCFF additionally unequipped for embedding complex logic functions. With a specific end goal to get an acceptable picture of the charge sharing in XCFF, it was re-enacted with distinctive installed capacities and the measure of most pessimistic scenario charge sharing was figured. The revised structure of the proposed dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Fig. 5. Note that in the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions.
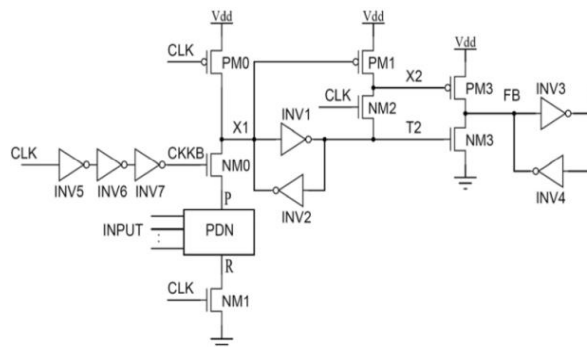

Figure 5: Block diagram of proposed DDFF-ELM

In the proposed structure [Fig. 5], since a low to high transition of CLKB occurs when CLK is low, the node $X1$ is held high by $PM0$ making this design free from charge sharing. The operation of the logic element is similar to the proposed DDFF. But, since CLKB is high during the pre charge phase, the drain diffusion capacitances of the "on" transistors in the PDN as well as that of $NM1$ would be charged high. Thus, during the low to high transition of the CLK, comparatively larger amount of charge has to be discharged before the voltage at X1 falls below the switching threshold of INV1–2. This may require a larger overlap period, which can be obtained by using a single inverter or a cascade of three inverters depending on the complexity of the incorporated logic as shown in Fig. 5. If Tvm is chosen for the worst case data transition in PDN, the analysis provided in (1) and (2) remains valid for the approximate estimation of the overlap period and hold-time for DDFF-ELM.

Reset Function

As far as synchronous designs are concerned, reset functionality is unavoidable. Here, we provide an area and power efficient method to incorporate asynchronous reset functionality to the proposed ELM. The ELM in Fig. 6(b) is modified to incorporate the active-low asynchronous-reset (rst_n) function by replacing the inverter pairs INV1-2 and INV3-4 with a NAND-based reset-circuit shown in Fig. 6(a).
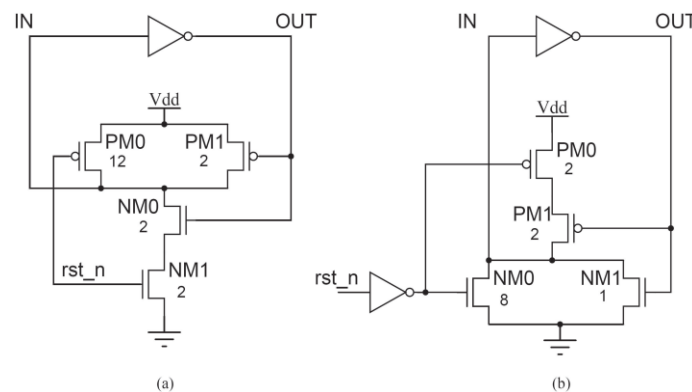

Figure 6: Incorporating asynchronous reset to logic embedded flip-flops.
(a) NAND-based reset circuit. (b) NOR-based reset-circuit.

Nodes IN and OUT of two reset-circuits replace the input and output of INV1 and INV3 of the ELM, respectively. Now, node X1 and QB are connected to IN and $X1B$ and Q are connected to OUT of the respective reset-circuits. The NAND-based reset-circuit operates as a cross-coupled inverter-pair when rst_n is high. On the negative edge of rst_n, $PM0$ pulls node $X1$ and QB high and reset is achieved. Larger width is used for $PM0$ to eliminate any power consumption resulting from contention when $X1$ or QB is pulled low during the reset period. Also, a large $PM0$ reduces the minimum width of rst_n signal, required to properly reset the flip-flop. Since $PM1$, $NM0$, and $NM1$ of Fig. 6 (a) are of minimum size, incorporating reset function induces a very low overhead in power and area.

Although the reset function has been incorporated only for DDFF-ELM, it is applicable equally well to the DDFF. The NOR-based reset-circuit acts as a cross-coupled inverter pair when rst_n is high, and on the negative edge of rst_n, $NM0$, pulls node $I N$ low to achieve the required reset. The inverter pairs INV1-2 and INV3-4 of SDFF [Fig. 6(a)] are replaced with NAND-based and NOR-based reset-circuits, respectively $NM0$ of the NOR-based reset-circuit is sized large to avoid any power consumption resulting from contention as explained earlier. A similar explanation carried out for the "reset" of proposed DDFF-ELM, when rst_n is held low for a small period of time. But, here [Fig. 6(a)] node X is pulled high and output Q is pulled low by the respective reset-circuits to achieve the reset operation.

C. 4-BIT UP-DOWN JOHNSON COUNTER

Counter is a device that stores the number of times a particular event or process has occurred often in relation to a clock signal. Counters are used in almost all the digital circuits for counting operations. A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.

The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using D- or JK-type flip-flops. The register cycles through a sequence of bit-patterns. The main advantage of the Johnson counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD. To initialize the operation of the Johnson counter, it is necessary to reset all flip-flops, as shown in figure 7.
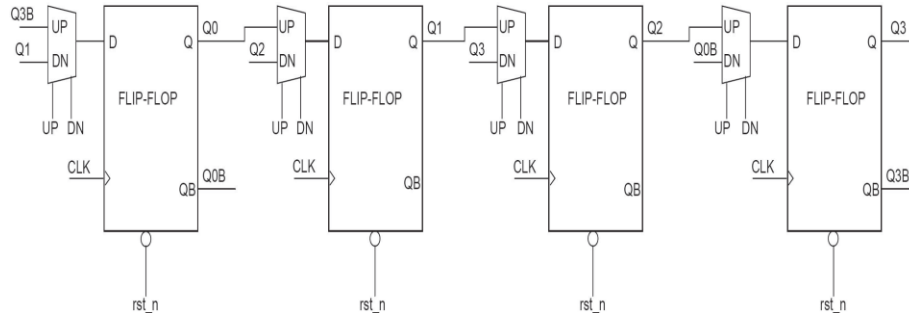
Figure 7 : 4-b Johnson up-down counter.

Figure 7 shows the architecture of 4-bit synchronous up-down Johnson counter. In Johnson counter output of the last stage is complemented and connected to the input of the first stage.

In the 4-bit up-down Johnson counter designed Dual dynamic pulsed hybrid flip-flop is used. By embedding a multiplexer into the flip-flop architecture counting operation can be performed in either up counting mode or down counting mode. Last stage output is complemented and connected to the input of the first stage for an up counter and first stage output is complemented and connected to last stage input as shown in the fig. 7. The counting sequence repeats for every eight clock pulses.

D. JOHNSON COUNTER WITH DML

The dual mode logic (DML) enables a very high level of energy-delay optimization flexibility at the gate level. In this paper, this flexibility is utilized to improve energy efficiency and performance of circuits. It can be switched between static and dynamic modes of operation according to system requirements and thus support applications in which a flexible workload is required as shown in Fig. 8. In the static mode, DML gates consume very low energy with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. The basic concept behind the DML is to combine the traditional CMOS logic (or any other static logic) with a dynamic logic. Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance). However, the dynamic mode is characterized by high performance with increased energy consumption (High Energy and High Performance).
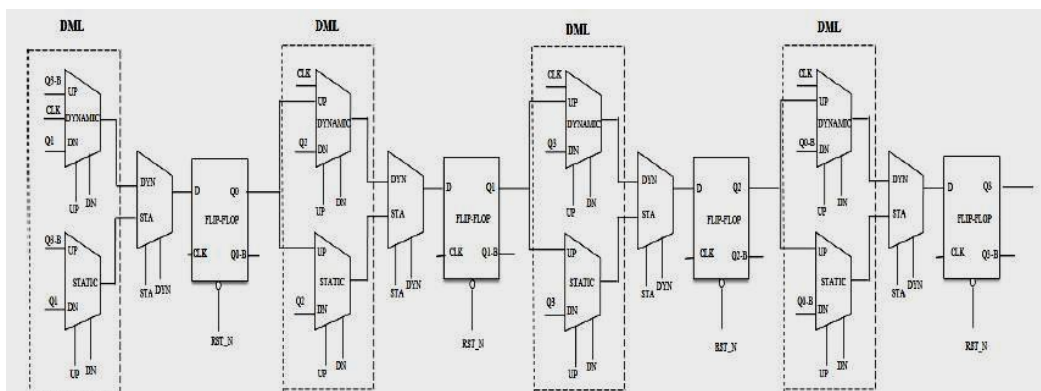

Figure 8: Johnson up/down counter with Dual Mode Logic

Figure 8 shows 4-b Johnson up/down counter comprises of four dual dynamic node pulsed hybrid flip-flops (DDFF) and DML multiplexers. The DDFF serves to be highly energy efficient with reduced delay. Initially all the flip-flops are in a reset condition. During up count, Q3-B is high („1") on both the static and dynamic multiplexers of DML. Depending on the mode of operation been selected through the selection lines (STA/DYN), inputs are given to the D-FF. Q0 is high („1") and passes onto the next DML part of the counter. Similarly the process continues depending on the counter operation (up/down).

Flip Flop	No. of Transistors	Data driving power (µw)	CLK driving power (µw)	Total power (µw)	Minimum Dq_ delay(ns)
Power pc 603	22	8.0212	6.4134	14.4346	32.6
SDFF	25	2.1103	16.131	18.241	19.8
HLFF	20	37.203	2.579	39.579	0.012
CDMFF	22	64.431	133.11	197.541	0.455
XCFF	21	14.839	7.210	22.049	0.341
Proposed DDFF	18	10.177	5.439	15.616	0.0977
Proposed DDFF-ELM	19	3.362	3.577	6.939	0.0174

Table 1 :Performance comparison of flip flop architectures

Embedded flip-flop	CLK power(µw)	Internal power(µw)	Total Power(µw)
DDFF-ELM	23.5	420.6	444.1

Table 2 : Performance of 4-b johnson up/down counter

Counter	Normal mux	DML MUX (Static)	DML MUX(Dynamic)
Power(µw)	1092	699	704
Delay(ps)	507	489	486

Table 3 : Performance analysis of 4-b johnson up-down counter with DML

IV. SIMULATION TEST BENCH

SIMULATION PARAMETERS

The existing and the proposed design are implemented in Tanner EDA tools in 90nm technology. Schematics for the design are designed in S-edit. The nominal supply voltage of the model is 1.2V. Measurements are made at different PVT conditions after postlayout parasitic extraction at respective temperatures. A load capacitance (CLOAD) of 50 fF is used in the test bench and a CLK frequency of 2 GHz is used in all the simulations. In order to estimate the three components of power in the flip-flops, the test bench used is shown in figure9.
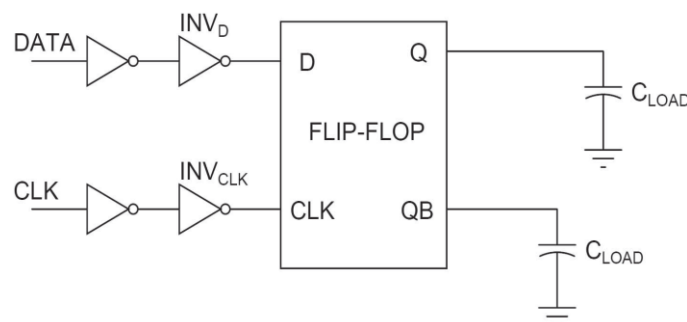

figure 9 : simulation test bench

The CLK driving power is found as the difference between power dissipated in the inverter (INVCLK) when loaded with the flip-flop and when not loaded with the flip-flop. Similar method is used to find the data driving power, where INVD is considered.

V. SIMULATION RESULTS

The existing and the proposed design are implemented in Tanner EDA tools in 90nm technology. Schematics for the design are designed in S-edit . Following figures shows the timing diagram of various flip flop designs simulated using T-spice and resulting waveforms are obtained in W-edit.

SIMULATION OUTPUT OF POWER PC
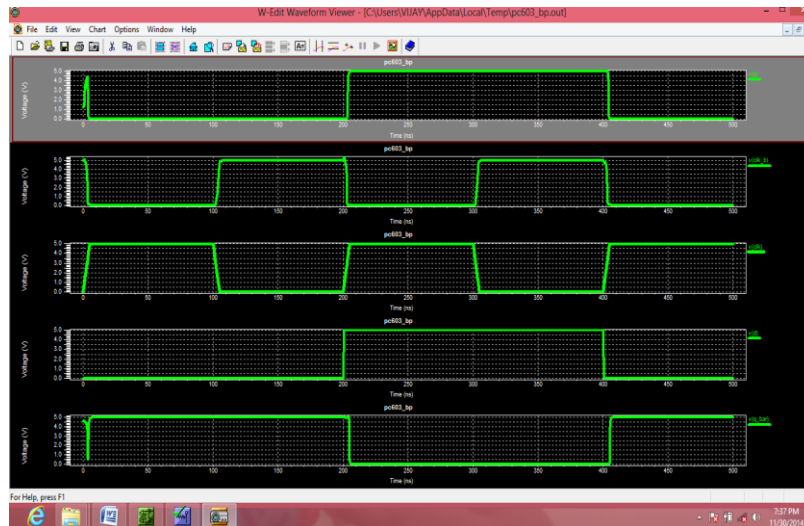
Figure (1): Simulation output of Power PC

SIMULATION OUTPUT OF SDFF
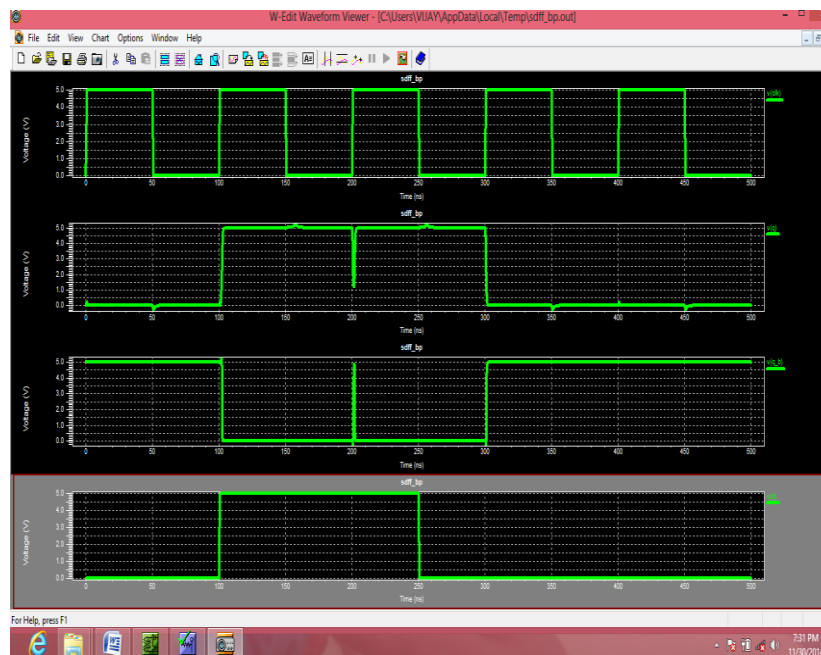
Figure (2) : Simulation output of SDFF

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SIMULATION OUTPUT OF HLFF
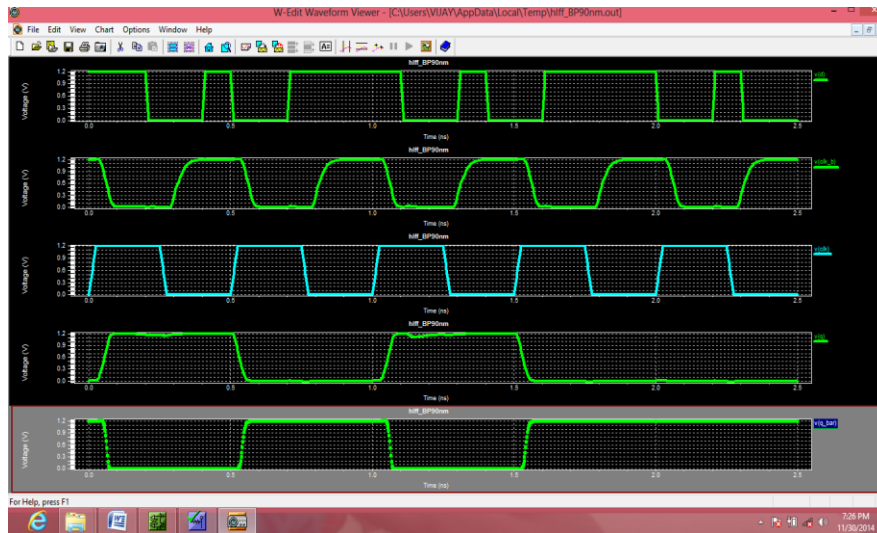
Figure (3): Simulation output of HLFF
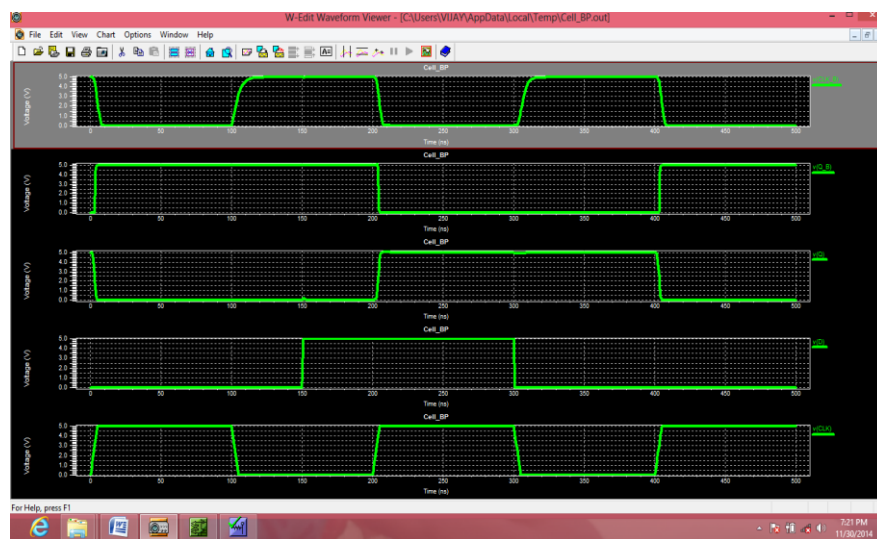
SIMULATION OUTPUT OF CDMFF

Figure (4) : Simulation output of CDMFF

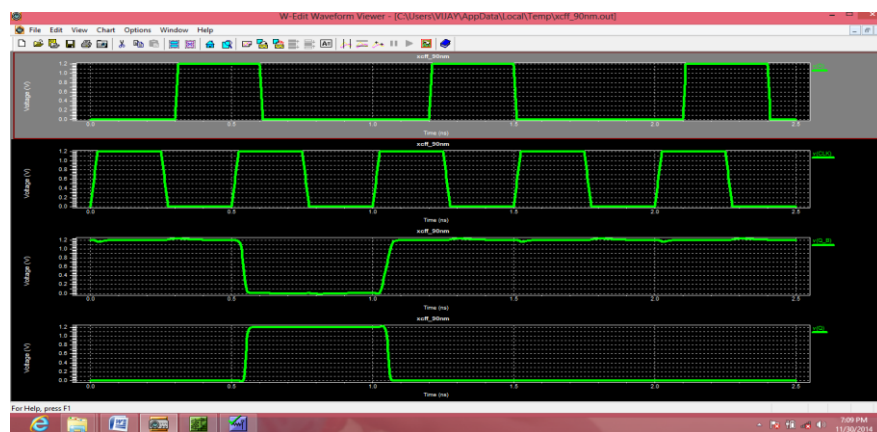**SIMULATION OUTPUT OF XCFF**

Figure (5): Simulation output of XCFF
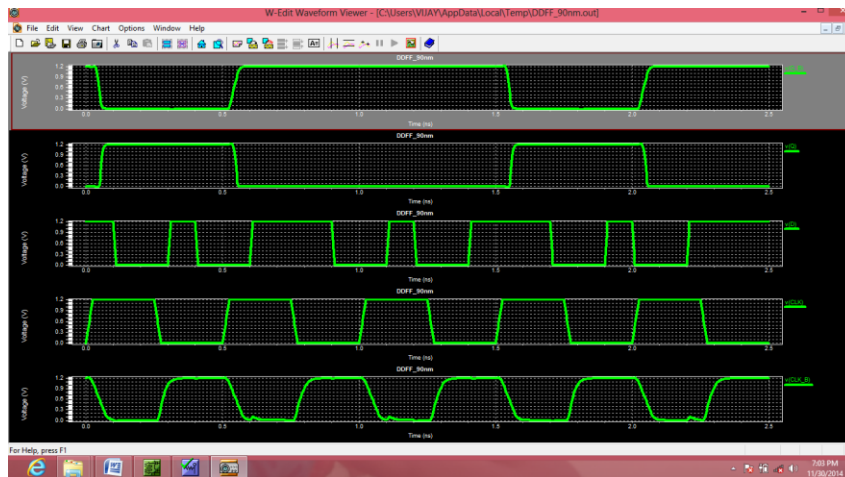
SIMULATION OUTPUT OF DDFF

Figure (6): Simulation output of DDFF
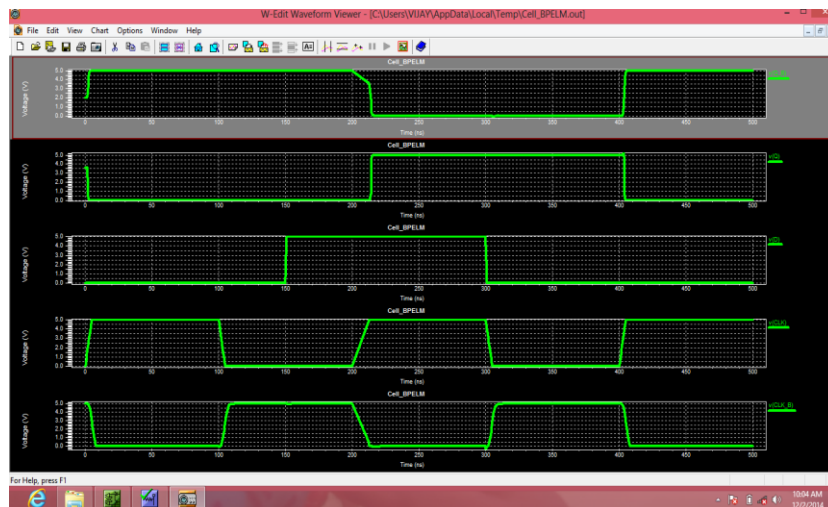
SIMULATION OUTPUT OF DDFF-ELM

Figure (7): Simulation output of DDFF-ELM

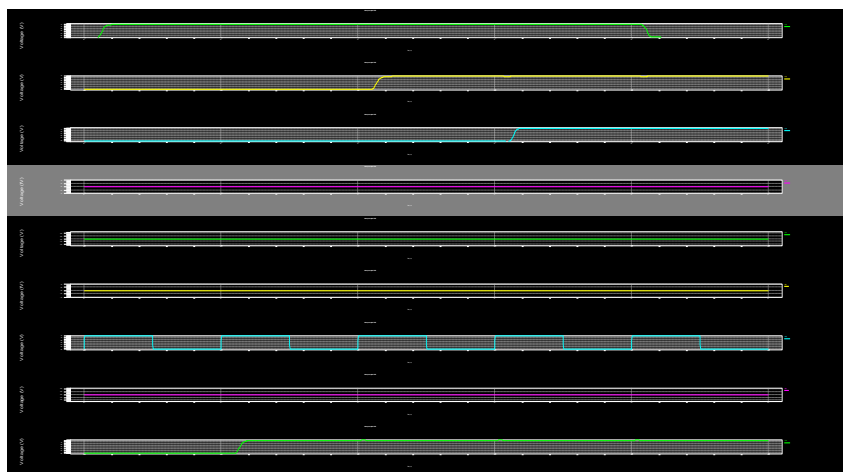## SIMULATION OUTPUTS OF JOHNSON COUNTER USING DML

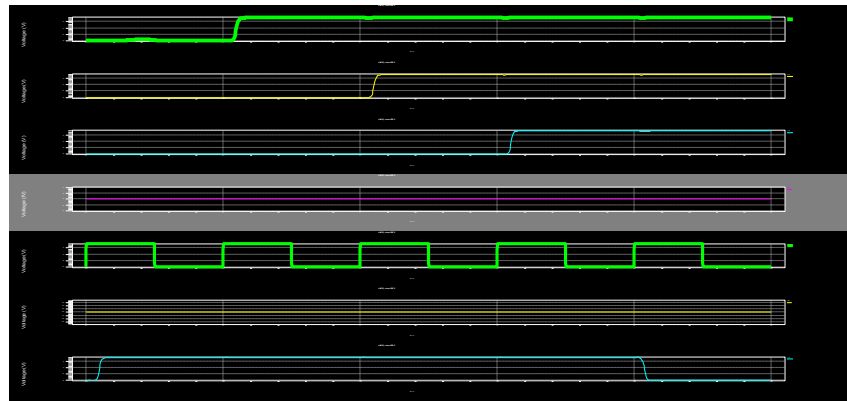**Figure (8):** 4-b Johnson up/down counter with normal multiplexer

Figure (9): 4-b Johnson up/down counter with DML (static) multiplexer
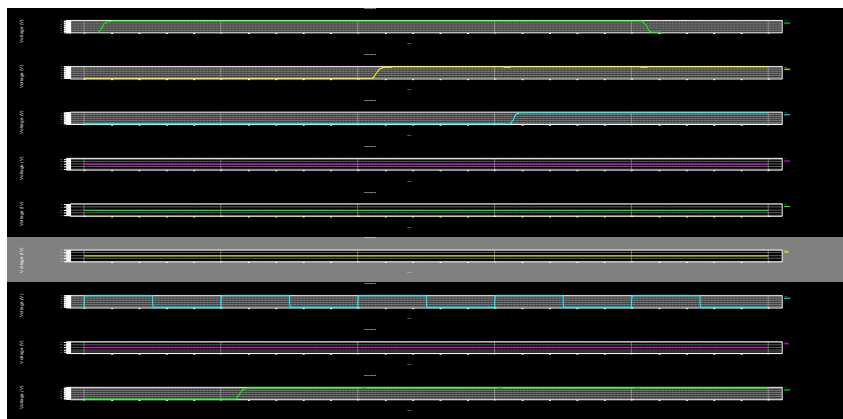

Figure (10): 4-b Johnson up/down counter with DML (dynamic) multiplexer

VI. CONCLUSION

In this paper, The DDFF eliminates the redundant power dissipation present in the XCFF.A comparison of the flip-flops showed that DDFF exhibits lower power dissipation along with comparable speed performances. Performance of a 4-b Johnson up-down counter with normal MUX and a 4-b Johnson up-down counter with DML logic were analyzed. DML logic can be switched between static and dynamic modes of operation according to the requirements of the system. Energy efficiency can be achieved by static DML mode and higher performance can be achieved by dynamic DML mode. The simulation result shows an improvement in power and delay parameters.

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