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A HIGH SPEED LOW POWER CAM AND TCAM WITH A PARITY BIT AND POWER GATED ML SENSING

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ABSTRACT

Content Addressable Memory (CAM) offers high-speed search function in a single clock cycle. Due to its parallel match-line comparison, CAM is power-hungry. Thus, robust, high-speed and sense amplifiers are highly sought-after in CAM In this paper, we introduce a parity bit that leads to 39% sensing delay reduction at a cost of less than 1% area and power overhead. We propose an effective gated-power technique to reduce the peak and average power consumption and enhance the robustness of the design against process variations. A feedback loop is employed to auto-turn off the power supply to the comparison elements and hence reduce the average power consumption by 64%. The proposed design can work at a supply voltage down to 0.5 V.A CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found and in some architectures, it also returns the data word, or other associated pieces of data. Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array. The extra circuitry also increases power searching speed cannot be accomplished using a less costly method.

Index terms: CAM, Amplifiers, Loop, Architectures.

I INTRODUCTION

Content addressable memory (CAM) is a type of solid-state memory in which data are accessed by their contents rather than physical locations. It receives input search data, i.e., a search word, and returns the address of a similar word that is stored in its data-bank .In general, a CAM has three operation modes: READ, WRITE, and COMPARE, among which “COMPARE” is the main operation as CAM rarely reads or writes [4]. Fig. 1(a) shows a simplified block diagram of a CAM core with an incorporated search data register and an output encoder. It starts a compare operation by loading an bit input search word into the search data register.The search data are then broadcast into the memory banks through pairs of complementary search-lines and directly compared with every bit of the stored words using comparison circuits. Each stored word has a that is shared between its bits to convey the comparison result. Location of the matched word will be identified by an output encoder, as shown in Fig. 1(a). During a pre-charge stage, the are held at ground voltage level while both and are at. During evaluation stage, complementary search data is broadcast to the and symbol. When mismatch occurs in any CAM cell (for example at the first cell of the row “1”; “0”; “1”; “0”), transistor and will be turned on, charging up the to a higher voltage level. A sense amplifier (MLSA) is used to detect the voltage change on the and amplifies it to a full CMOS voltage output. If mismatch happens to none of the cells on a row, no charge up path will be formed and the voltage on the will remain unchanged, indicating a match.

Since all available words in the CAMs are compared in parallel, result can be obtained in a single clock cycle.

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Hence, CAMs are faster than other hardware- and software-based search systems [1]. They are therefore preferred in high-throughput applications such as network routers and data compressors. However, the full parallel search operation leads to critical challenges in designing a low-power system for high-speed high-capacity CAMs [1]: 1) the power hungry nature due to the high switching activity of the and the and 2) a huge surge-on current (i.e., peak current) occurs at the beginning of the search operation due to the concurrent evaluation of the may cause a serious IR drop on the power grid, thus affecting the opera tional reliability of the chip [1]. As a result, numerous efforts have been put forth to reduce both the peak and the total dynamic power consumption of the CAMs [2]–[8]. For example, Zukowski *et al.* and Pagiamtzis *et al.* introduced selective pre-charge and pipe-line architecture, respectively to reduce the peak and average power consumption of the CAM [8]. [5], [6] and [3] utilized the precharge low scheme (i.e., low swing) to reduce the average power consumption. These designs however are sensitive to process and supply voltage variations. As will be shown later in Section IV, they can hardly be scaled down to sub-65-nm CMOS process. In this work, a parity-bit is introduced to boost the search speed of the parallel CAM with less than 1% power and area overhead. Con- currently, a power-gated sense amplifier is proposed to improve the performance of the CAM comparison in terms of power and robustness. It also reduces the peak turn-on current at the beginning of each search cycle. The rest of paper is organized as follows. Section II introduces parity-bit based CAM architecture. In Section III, the gated- power technique is proposed. Performance analysis are presented in Section IV. Section V concludes this paper.

II PROBLEM AND ANALYSIS

SEARCH SPEED BOOST USING A PARITY BIT

We introduce a versatile auxiliary bit to boost the search speed of the CAM at the cost of less than 1% are overhead and power consumption. CAM at the cost of less than 1% area and power consumption.

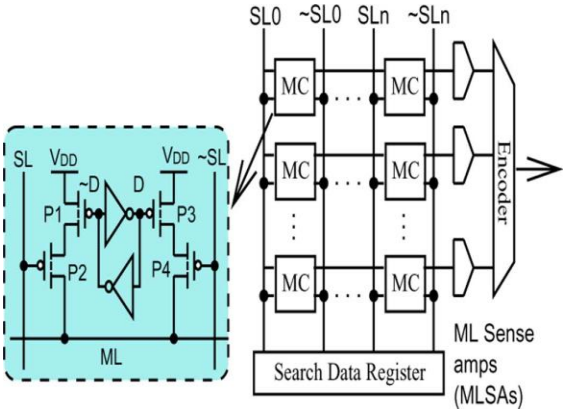

Fig 1. Block diagram of conventional CAM

PRE-COMPUTATION CAM DESIGN:

The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison. These extra bits are derived from the data bits and are used as the first comparison stage. For example, in Fig. 2(a) number of "1" in the stored words are counted and kept in the *Counting bits* segment. When a search operation starts, number of "1"s in the search word is counted and stored to the segment on the left of Fig. 2(a). These extra information are compared first and only those that have the same number of "1"s (e.g., the second and the fourth) are turned on in the second sensing stage for further comparison. This scheme reduces a significant amount of power required for data comparison, statistically. The main design idea is to use additional silicon area and search delay to reduce energy consumption.

The previously mentioned pre-computation and all other existing de- signs shares one similar property. The sense amplifier essentially has to distinguish between the matched and the 1-mismatch . This makes CAM designs sooner or latter face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. This problem is usually referred to as. Thus, we propose a new auxiliary bit that can concurrently boost the sensing speed of the and at the same time improve the of the CAM by two times.

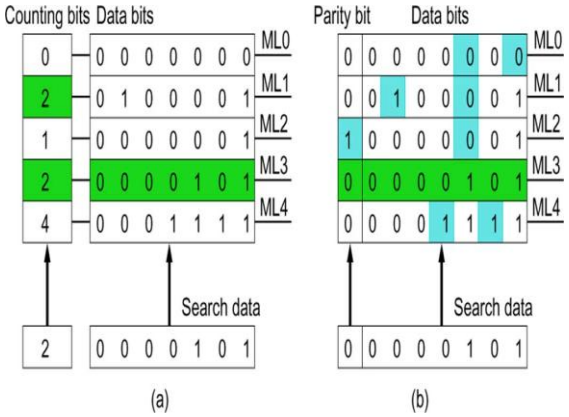

Fig 2.a) Conventional CAM, b) proposed parity bit based CAM

PARITY BIT BASED CAM

The parity bit based CAM design is shown in Fig. 2(b) consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below. In the case of a matched in the data segment, the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment, the parity bits are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only have to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed design greatly improves the search speed and the ratio of the design. Fig. 3 shows the 1-mismatch transient waveforms of the original and the proposed architecture during the search operation. In Section III, we are going to proposed a new sense amplifier that reduces the power consumption of the CAM.

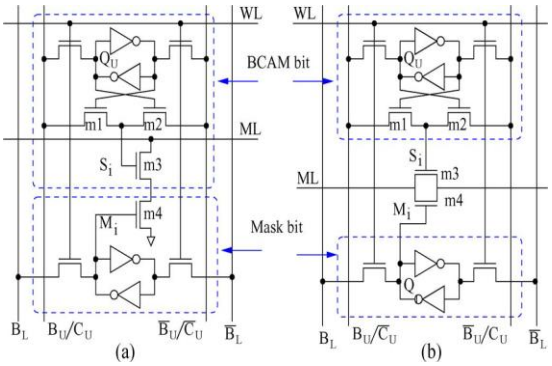

Fig 3.Circuit diagram of TCAM

POWER GATED ML SENSE AMPLIFIER DESIGN

OPERATING PRINCIPLE

The proposed CAM architecture is depicted in Fig. 4. The CAM cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NOR CAM (shown in Fig. 1) and use a similar structure. However, the "COMPARISON"unit, i.e., transistors, and the "SRAM" unit, i.e., the cross-coupled inverters, are powered by two separate metal rails, namely and the respectively. The is independently controlled by a power transistor and a feedback loop that can auto turn-off the current to save power. The purpose of having two separate power rails of is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle. As shown in Fig. 4, the gated-power transistor is controlled by a feedback loop, denoted as "Power Control" which will automatically turn off once the voltage on the reaches a certain threshold. At the beginning of each cycle, the is first initialized by a global control signal . At this time, signal is set to low and the power transistor is turned. This will make the signal and initialized to ground and ,respectively. After that, signal turns *HIGH* and initiates the COMPARE phase. If one or more mismatches happen in the CAM cells, the will be charged up. Interestingly, all the cells of a row will share the limited current offered by the transistor, despite whatever number of mismatches. When the voltage of the reaches the threshold voltage of transistor voltage at node will be pulled down. After a certain but very minor delay, the NAND2 gate will be toggled and thus the power transistor is turned off again. As a result, the

is not fully charged to but limited to some voltage slightly above the threshold voltage of M8, shows the simulation result of the proposed power controller. One can see that, the slopes of the node and node depend on the number of mismatches. When more mismatches happen (e.g., 128 in the simulation), the and change faster. Less number of mismatches (e.g., 1 in the simulation) will slow down the transition of node and results in a longer delay to turn off transistor).

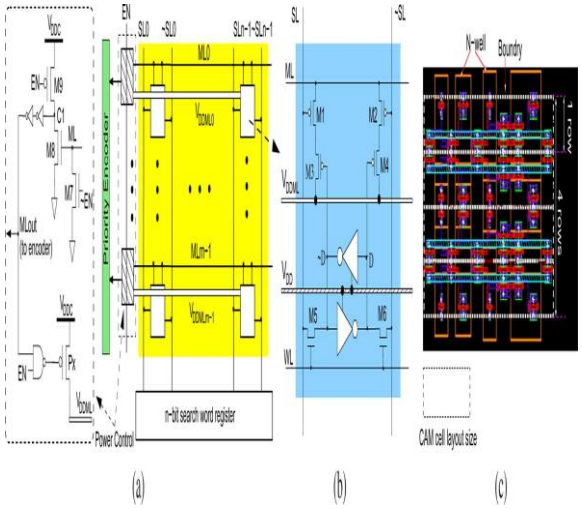

Fig 4. Proposed CAM Architecture

A cam with a power transistor strength of the 1mismatch case is about 10% weaker than that of the conven tional design and thus slower. However, as we combine this sense amplifier with the parity bit scheme mentioned in Section II, the overall search delay is improved by 39%. Thus the new CAM architecture of- fers both low-power and high-speed operation.

CAM CELL LAYOUT

The layout of the CAM cell using 65-nm CMOS process. Since the new CAM cell has a similar topology of that of the conven- tional design (except the routing of their layouts are also similar. These two cell layouts have the same length but different heights. In the new architecture, cannot be shared between two adjacent rows, resulting in a taller cell layout, which incurs about 11% area overhead, as shown in Fig. 6.

PERFORMANCE COMPARISONS

In this section, performance of the proposed design will be evaluated using the conventional circuit and those in [5], [6] as references. In [5], the power consumption is limited by the amount of charge injected to the at the beginning of the search. In [6], a similar concept is utilized with a positive feedback loop to boost the sensing speed. Both designs are very power efficient. As will be shown latter, the proposed design consumes slightly higher power consumption when compared with [5] and [6] but is more robust against PVT variations.

PEAK CURRENT AND IR DROP ATTENUATION

The proposed power controller demonstrates a great reduction in the transient peak current. This can be explained by the bottleneck effect of transistor .shows the transient current as a function of the number of mismatches occurring in a row of 128 CAM cells during the COM- PARE cycle of the proposed and the conventional designs. The conventional design's peak current increases almost linearly from 25 A (1 mismatch) to 1.45 mA (64 mismatches) and finally 2.8 mA (128 mismatches). Although the overall transient charge up current of the proposed design also increases with the number of mismatches, it will soon reach its limit due to the presence of the gated-power transistor For instance, when 128 mismatches occurs, the peak current is capped at 155 A, which is less than eight times as compared to the case when only one mismatch occurs (i.e., 21 A).swing on the bus. Another contributing factor to the reduced average power consumption is that the new design does not need to pre- charge the buses because the EN signal turns off transistor of each row and hence the buses do not need to be pre-charged, which in turn saves 50% power on the buses .illustrates the average energy consumption (divided into power and power) of the proposed design as compared to other three benchmark designs, including all the power overhead of the control circuitry.

Since [5], [6], and the proposed design do not precharge the before each compare cycle, their energy consumption is only half of that of the conventional circuit. As for the energy, at 1V supply voltage the proposed design only dissipates 0.41 fJ/search/bit while that of the conventional design is 1.148 fJ/search/bit. Our energy consumption is higher than that of [5] (10.8%) and [6] (32%) but as will be shown below, our proposed design is much more robust against process and environment variations. consumption. This is mainly due to the reduced voltage

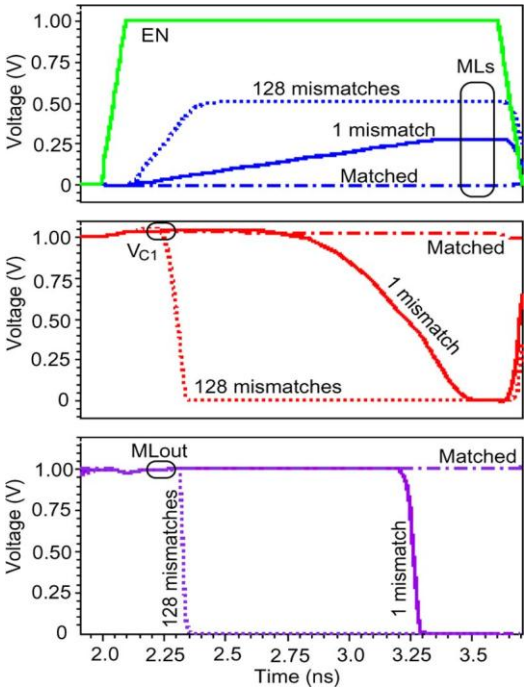

Fig 5. Three rows of 128 bit proposed design

This drastic reduction in the peak current translates to a vast improvement in operation reliability. Our simulation result has shown that for a CAM array implemented in a 65-nm CMOS process, the worst-case IR drop at the center of the conventional CAM can be as large as 0.18 V (i.e.,18%) while that of the proposed design is only 8 mV (i.e., 0.8%). Also, it only requires the net to have a width of only 150 nm instead of 2 m vertical. The new vertical now only supply the leakage current to the SRAM cell and thus does not require a large metal width.

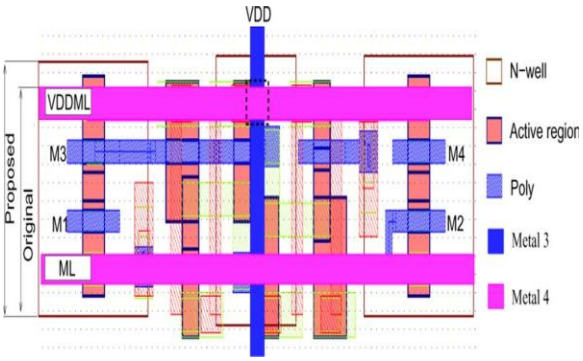

Fig 6.Layout of the proposed CAM cell

DYNAMIC POWER CONSUMPTION

Because the power-gated transistor is turned off after the output is obtained at the sense amplifier, the proposed technique renders a lower average power

SUPPLY VOLTAGE SCALINGS

We investigate the ability of the four designs to work at low supply voltage, by re-implementing the designs in [5], [6] and the conventional one into the same 65-nm technology. Designs in [5] and [6] demonstrate poor adaptability to voltage scaling. They cannot operate already launched s supply voltage lower than 0.9 V. On the contrary, when the supply voltage scales to 0.5 V, both the proposed and the conventional design can work well. First, the search energy of the four designs in consideration is presented in Fig. 9(a). It can be seen that at 1 V supply voltage, [5] and [6] have the lowest energy consumption per search, followed by the pro- posed design. However, they cease to work when the supply voltage scales down to below 0.9 V. Between the conventional and the proposed design, the proposed design consumes 62% less power consumption at any supply voltage value. Second, the sensing delay comparison is shown in Fig. 9 where the proposed design has 39% improvement when compared to the conventional design and is the fastest de- sign. This figure also suggests that sensing delay increases dramatically when supply voltage enters the near-subthreshold region. Finally, the corresponding leakage currents of the four designs against voltage scaling is are shown in Fig.

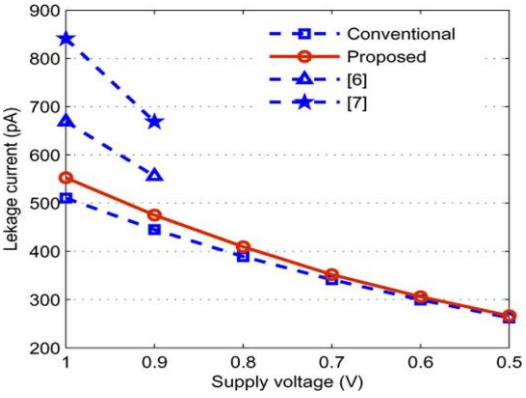

Fig 6. Leakage current of four designs

The proposed design is the second-best circuit after the conventional design. Both of them have about 20% and 37% lower leakage current when compared to [5] and [6] at 1 V, respectively. This feature confirms that the proposed design is more suitable for ultra-low power applications in 65-nm CMOS process and beyond.

TEMPERATURE VARIATIONS

We also carry out the temperature variation analysis on the four de- signs (see Fig. 11). It can be seen that the [6] is the most vulnerable design and thus can only work in a narrow range of temperature variation. [5] can work through out the whole temperature range but having more than 30% speed fluctuation. In contrast, the proposed and the conventional design are much more stable with less than 4% sensing delay variation.

B. PROCESS VARIATIONS ANALYSIS

Process variation is a critical issue in nanoscale CMOS technologies. We simulate the performance of the proposed design against empirical process variation data from the foundry. It is worth mentioning here that the feedback loop to turn off the gated-power transistor operates digitally and hence is almost insensitive to process variations. Similar to the conventional design, there are two scenarios where the proposed design may sense the results wrongly: 1) the sense amplifier is enabled too early, the 1-mismatch has not been pulled up to a voltage higher than the threshold value and thus trigger the output in- verter and 2) the delay of the enable signal is too long, resulting in the matched to be pulled up by the leakage current, indicating wrong miss. We use 50000-cycle Monte Carlo simulations on these designs at different supply voltages and count the number of errors accordingly.

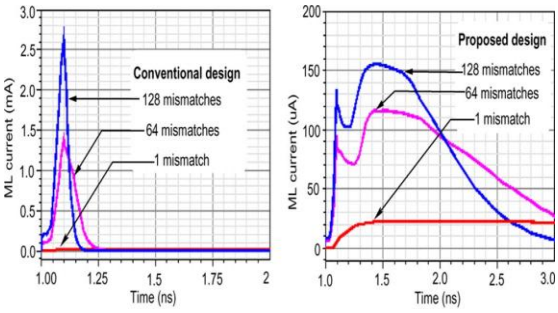

Fig 7. Simulated transient current

The [5] and [6] are very sensitive to process variations with more than1000 and 10 000 errors count, respectively. Also, they stop working at 0.9 V supply. On the contrary, the proposed and the conventional de- sign has no sensing error even if scales down to 0.7 V. At lower supply voltage, the conventional design continues to work 100% correctly while the proposed design has 51 and 298 error counts at 0.6 and 0.5 V, respectively.

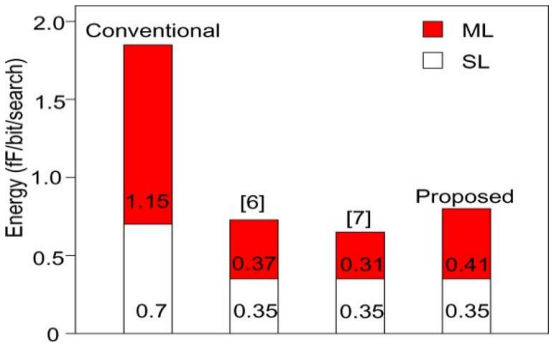

Fig 8. Total average power consumption

This is because both designs operates at the same frequency but the proposed design has a smaller pull-up current due to the gated-power transistor and hence some times error happens. We have carried out a separate simulation for the proposed design with a slightly slower frequency and has confirmed that no error occurs. It is worth mentioning here that extending the period for [5] and [6] does not result in any error count reduction since these designs are based on feedback loop structure and decisions are made at the very beginning of the sensing cycle.

III CONCLUSION

We proposed an effective gated-power technique and a parity-bit based architecture that offer several major advantages, namely reduced peak current (and thus IR drop), average power consumption (36%), boosted search speed (39%) and improved process variation tolerance. It is much more stable than recently published designs while maintain their low-power consumption property. When compared to the conventional design, its stability is degraded by 0.6% only at extremely low supply voltages. At 1 V operating condition, both designs are equally stable with no sensing errors, according to our Monte Carlo simulations. Its area overhead is about 11%. It is therefore the most suitable design for implementing high capacity parallel CAM in sub-65-nm CMOS technologies.

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